



V9050 USB 2.0 Device Core



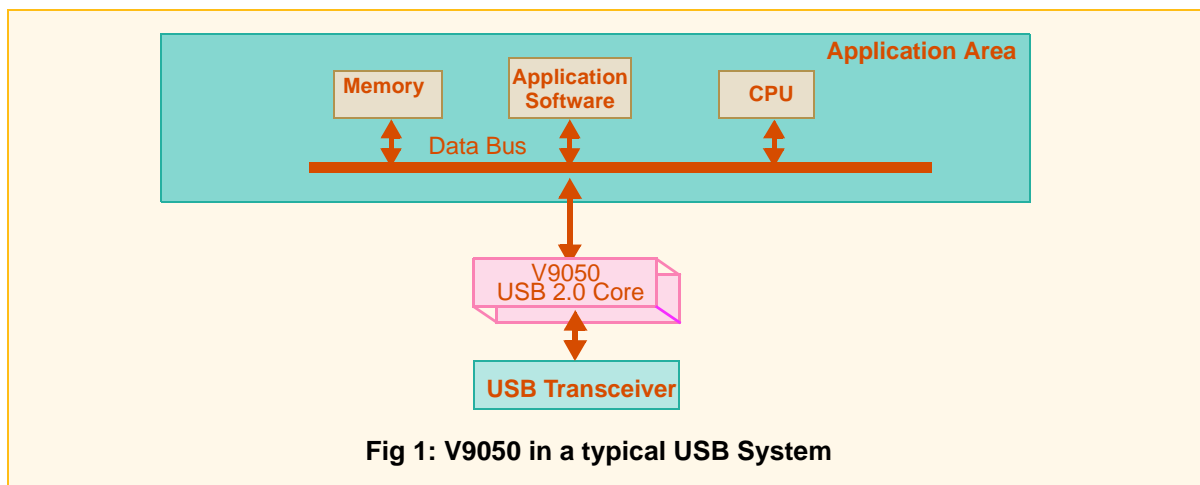
Features

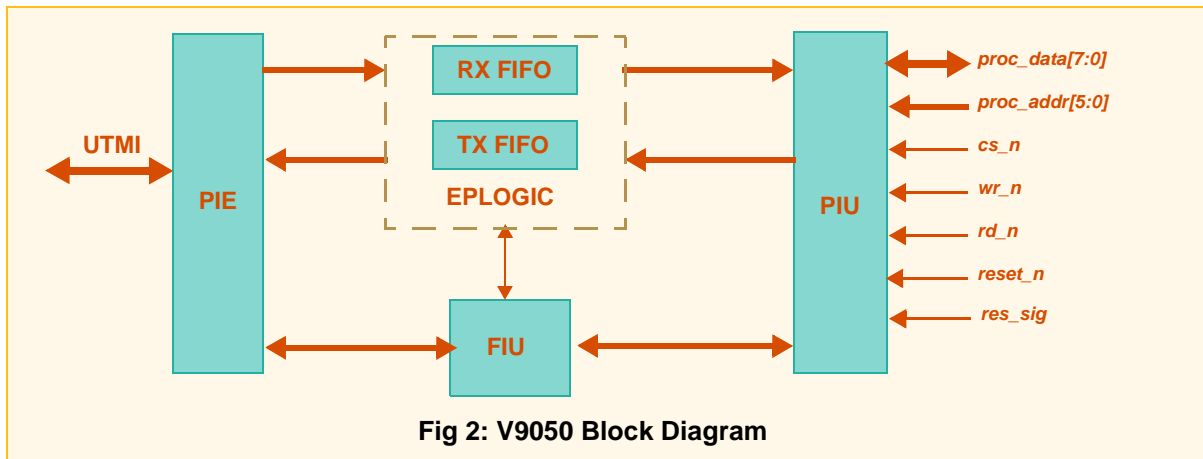
- Complies with USB Specification Revision 2.0
- PHY interface compliant with UTMI Specification, Version 1.05
- Supports USB defined high-speed (480 Mbps) and full-speed (12 Mbps) operation
- Supports USB defined Remote Wake-up capability
- Interfaces with most of the microcontrollers and microprocessors
- Megacell requests to CPU are interrupt driven to minimize the polling time requirements
- Facility to program endpoint as interrupt or bulk

Functional Overview

The V9050 megacell is a USB 2.0 device core that can be integrated with hardware of any peripheral device resulting in a peripheral with USB interface capability. The core provides all the functionality at the physical level (digital) and transaction layers of the USB specification. The core provides a high-level user interface, shielding the user from USB protocol details. Automatic data retry is supported in the core and is not passed on to the higher level software layers. The megacell in a typical USB system is shown in Fig 1: V9050 in a typical USB System.

The megacell interfaces externally with UTMI compatible PHY chip on one side and with any industry standard microcontroller/microprocessor on the other side. The major blocks are the PIE, FIU, FIFO and PIU. The PIE block generates CRC on the data to be transmitted and on the received data it checks for CRC match, any packet errors. The FIU handles the proper routing of data to/ from the endpoint FIFO's. The FIFO block holds the logic necessary for controlling RAM for different endpoints. The RAM can be shared among different endpoints, thereby conserving area. Apart from default endpoint EP0, the core supports bi-directional endpoints EP1 and EP2, which can be programmed for either interrupt or bulk type of data. The PIU block holds the logic necessary for interfacing with any generic microcontroller/ processor. The address, data and control signals are synchronized within the core. The megacell block diagram is shown in Fig 2: V9050 Block Diagram.





Performance Specifications

Parameter	Value	Remarks
Gate Count	13.5k	Excluding RAM
Code Coverage	100%	Using SureCov tool
Technology	0.18m	artisan tsmc
Frequency	45Mhz	16-bit interface on PHY side

Target Applications

- This core is designed to meet the needs of any application that can work on USB 2.0 specification like digital video cameras, DSL modems, High quality audio systems, video conferencing
- The core can be used in SoC designs for embedded applications which require USB interface

Test Coverage

- Scan insertion is performed using Mentor DFT Advisor
- The ATPG vectors are generated using Mentor Fast Scan and fault coverage of 96% is obtained
- MBIST Architect from Mentor Graphics is used to test the memory

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data sheet, User Guide
- Synthesis Scripts & Timing Constraint files
- Scripts for STA

- Scripts for DFT (Optional)
- Verification Suite

Additional Items

- USB Client Software Driver development - order based

Related Products

- V9012P USB 1.10 Device Core (Full-speed)
- V9006 USB 1.10 Device Core (Low-speed)
- V9030 USB 1.10 Hub Core
- v9050ocp USB 2.0 device with OCP interface

QCL_10009_DF_02_Data Sheet_Rev100

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