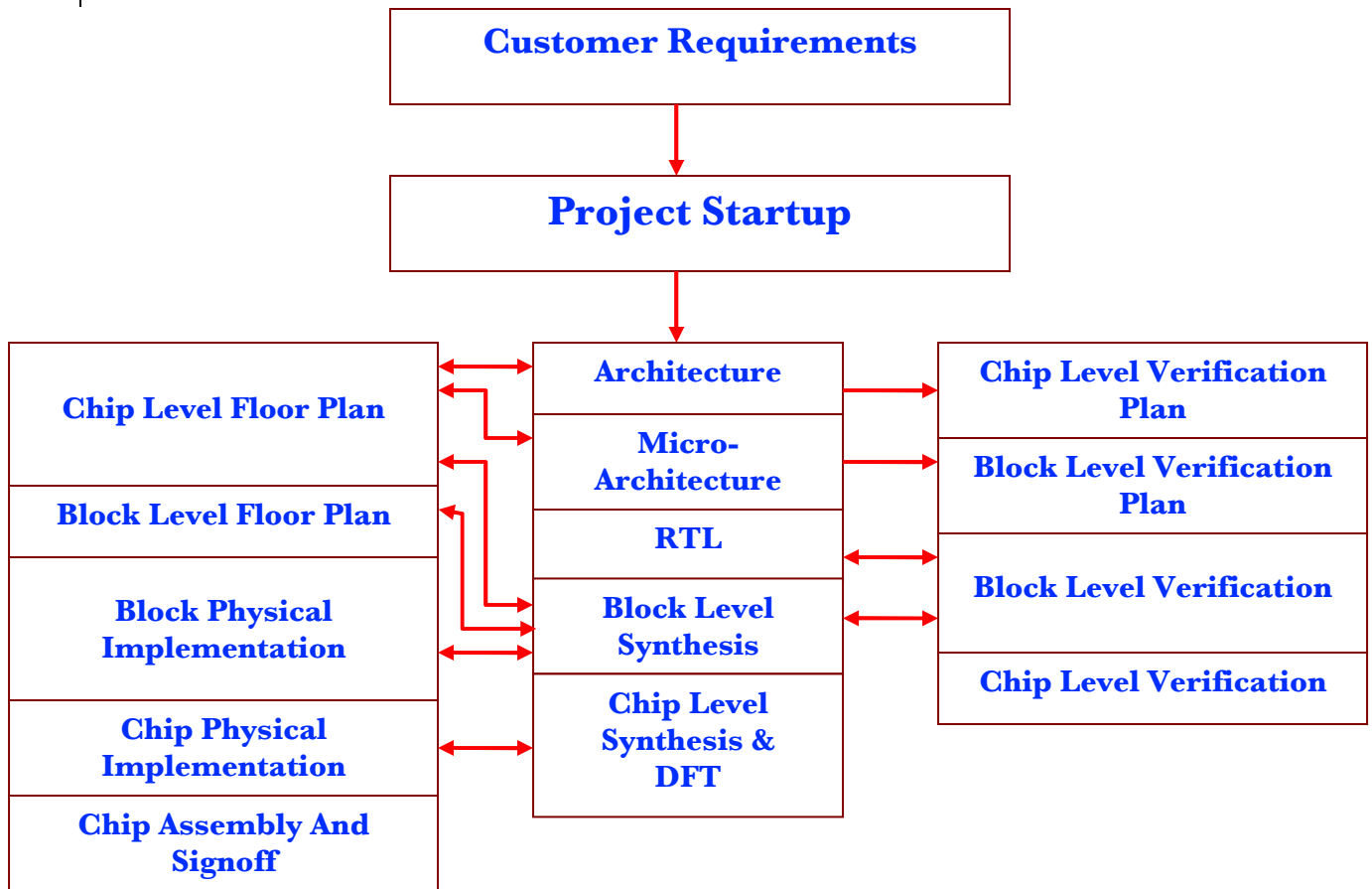


QualCore SOC Flow



SOC Flow Overview



Today's complex designs, especially those targeted to deep submicron technologies, demand a good methodology at all stages of the design cycle in order to meet the quick turnaround requirements of customers. A good methodology is one of the major contributing factors to first spin success.

QualCore has an established design flow, refined over a several customer projects, which ensures a quick turnaround from concept to silicon. QualCore has an established QC process throughout the design flow with audit & review mechanisms that guarantee consistent quality and fast turnarounds. This document briefly outlines salient features in QualCore's design flow

Project Startup

- Capture customer requirements and list down all the required features
- Identify the components and interfaces for getting the required functionality and performance. This task typically requires study of different standards and protocols.
- Come up with a top level block diagram
- Project plan draft – Document clearly mentioning manpower, hardware resource requirements, tools requirement, tentative schedules & risks, macros sourcing, functional & performance goals, operating modes, Overall flow for executing the project and deliverables.
- Project plan sign-off from customer
- Identify single-point-of-contact on customer and QualCore side for clarifications

Architecture

- Translate functional requirement to architecture. Comprises design partitioning, I/O interface definition, clock & reset strategy, software interface, internal bus selection and data flow diagrams to assist the initial floor plan task
- Detailed specifications of high-level blocks in QualCore's well-defined formats. Architecture specification document to guide all further steps
- Comprehensive audit & review: Review by project manager, independent auditor, project lead, verification lead and backend lead. Review focus is to see that architecture meets the functional and a performance goal, specification document is complete and architecture allows verifiability of design. QualCore's detailed audit checklist guide the review process
- Architecture Specification document sign-off by Project Manager and Independent Auditor

Chip Level Verification Plan

- Verification of chip-level functionality using a black box approach
- QualCore's clearly defined knowledge/specifications on transfer documents facilitate quick ramp up of verification team. The interface documents comprehensively outline chip specifications, protocols, I/O specifications and exception conditions
- Definition of chip level verification environment and test cases. QualCore's large portfolio of reusable verification components is leveraged to reduce verification effort. Tests include functional tests, directed random tests and regression tests. Coverage of > 90% is targeted.

- Audit and Review team checks the verification plan document for completeness and implementability of verification plan. The verification bench should facilitate the checking of all the listed features of the chip, it should have a way to automatically monitor and check the performance goals like throughput

Micro-Architecture

- Detailed design of individual blocks: Block level I/O & timings definition, algorithms & state machines definition, data paths and control path design, specification of synchronization requirements. Preparation of MA specification document is facilitated by QualCore's standard templates & checklists
- Estimation of memory resources and gate count
- Elaboration of register bit definitions corresponding to each block
- Clock and reset design as per the clock & reset strategy defined in the architecture specification document
- Micro-Architecture Specification document sign-off by Project Manager and Independent Auditor. The main checks include design choice correctness and compliance of functionality & timings

Block Level Verification Plan

- Verification plan of individual blocks using a white-box approach. The document includes verification environment, test cases, stimulus application mechanism & response checking, plan for random checks, use of reusable components
- The Architecture & Micro Architecture specs documents are used as a reference to list out critical and corner cases. 100% code coverage is targeted
- QualCore's comprehensive guidelines & templates aid planning
- Audit and Review team checks the document for completeness and implementability of verification plan

RTL

- QualCore's directory structure guidelines and automation scripts ensure quick ramp up
- RTL coding for each block in Verilog/VHDL. QualCore's customer specific coding guidelines are strictly followed. Parametrization, synchronous design, avoiding usage of scripts related to a particular synthesis tool in the RTL are some of the key guidelines in creating a reusable code
- Linting (using SureLint) for each block to ensure the code is lint free. In addition, code walk through to ensure the coding is done efficiently
- Boundary Scan & MBIST are inserted
- Block level logic is integrated to get top-level RTL files. QualCore's utilities, VPP & RTL Gen, are used to integrate the blocks
- Linting is again done on integrated code
- Systematic backups and version control processes to ensure code safety & integrity

Block-Level Verification

- Test benches and test vectors are developed as per Block-Level Verification document. Functional verification is carried out and any bugs reported, followed by directed random tests, regression tests and code coverage analysis (using Sure Cover)
- Adoption of advanced verification tools (Vera) currently in pipeline
- Audit and Review team checks if test bench is as per plan document, examines reasons for modifications or additions, examines whether coverage is achieved and reasons for variance, checks whether the targeted coverage is achieved.
- Systematic backups of test-benches and version control processes to ensure code safety & integrity.

DFT

- MBIST and boundary scan are done at the RTL step itself
- Scan violations check at block level and chip level using DFT compiler with rtdrc
- Scan Insertion at block level
- Chip level scan chain stitching
- ATPG vectors are generated using Mentor's FastScan and ATPG vectors are verified

Chip Level Verification

- Chip level verification after all blocks of SoC are integrated DUT is mounted on test bench and test cases are applied
- Sanity checks are done for checking interconnectivity between blocks and then all the functional tests are run followed by constrained random tests and regression tests.
- Audit & Review team checks coverage results and signs-off the RTL

Chip Level Floor Plan

- This is a critical step as it not only defines the layout of the chip but also provides preliminary wireload models and parasitic estimates to the Synthesis step, required for constraining the block-level netlist. QualCore uses Cadence First Encounter for chip level floor planning
- Most physical design activities, including floor planning, are very involved and comprise numerous discrete activities. QualCore manages efficient execution through clear guidelines, checklist and sign-off process
- The various activities in QualCore's floor planning step include
 - **Die Size estimation** using QualCore's in-house tools
 - **Power planning:** Power/ground pads placement and power mesh structure
 - **IO placement** based on information from front-end team
 - **Virtual Prototyping** for early feasibility analysis of netlist, floor plan and constraints
 - **Block & hard macro placement** based on virtual prototyping or designer inputs

□ **Bus and clock pin placement**

Synthesis

- QualCore's has a robust synthesis and physical design flow, which has been extensively tried and tested in several multi-million gate projects in 0.13 μ and 0.18 μ with aggressive timing & power requirements. Besides, most of the projects were completed on fast-track schedules owing to QualCore's well-established processes
- QualCore uses Synopsys DC for synthesis. Design productivity is improved through script templates for all tasks
- Various steps typically involved in QualCore's synthesis flow include:
 - **Library inspection:** Consistency check between different views and availability checks of required cells
 - **Design Exploration:** Synthesis lint checks and acceptance of directives
 - **Chip Level Floor Plan:** Executed by physical design team to provide wireload models, inter-block wire lengths and parasitics for block constraint definition
 - **Constraint definition:** Block level i/o, clock definition, identification of high fan-out, identifying timing exceptions
 - **Preliminary Synthesis(1st Pass):** Synthesis and integration of all blocks
 - **WLM and Parasitic extraction:** Place & Route of Netlist and extraction of wireload models and parasitics for synthesis. Executed by physical design team.
 - **Design budgeting:** Refine constraints based on parasitics & wire delays from previous step and to accommodate for inter-block logic
 - **Optimization:** Block-level synthesis & optimization, integration of blocks, incremental compile to meet block to block delays
 - **Equivalence check between RTL and Netlist**
 - **Static Timing Analysis:** Timing & EDRC analysis using sign-off timing analysis tool. In case of any timing violations, IPO(In place Optimization) is done or Physical Design team fixes the violations using physical knowledgeable synthesis tools

Block Level Floor Plan

- QualCore uses Cadence First Encounter, Mentor Graphics Calibre, Cadence Layout Plus
- Typical tasks in QualCore's flow include – Fine adjustments to macro locations, pin locations and power mesh to meet critical timing requirements or create spacing, Pre-placement of timing critical cells and power plan verification

Block Physical Implementation

- QualCore's flow uses hierarchical place & route
- Tools used in QualCore's flow are Cadence SOC Encounter, Cadence PKS, Cadence Fire & Ice QX, Synopsys Prime Time Timing Analyzer, Mentor Graphics Calibre and Cadence LayoutPlus. In addition, QualCore has checklists for each step and at the end of each step an audit of logs is done for early detection of errors
- Typical steps involved in QualCore's flow include:

- Trial Place & route for feasibility check
- Placement & scan reorder
- High fanout net and clock tree synthesis
- Hold time analysis and fix
- Crosstalk analysis and fix
- Fixes for Electro-migration, manufacturing yield enhancement and process antenna violation
- Dummy metal insertion to meet minimal metal density of foundry
- 3D parasitic extraction for timing analysis.
- Power, Crosstalk and IR drop analysis; power plan alterations in case of violations
- Physical verification: Block GDSII merged with cell GDSII to provide block merged GDSII. DRC, LVS and ANT checks on block merged GDSII.
- Timing, Power, Noise and Abstract view generation
- Block GDSII and Parasitics are passed to the front end team who perform Formal Verification using Synopsys Formality and STA using Synopsys Prime Time

Chip Physical Implementation

- This step uses the abstract views of all the blocks and does a chip level place & route.
- Tools used by Qualcomm in this step are Cadence SOC Encounter, Cadence PKS, Cadence Fire & Ice QX, Synopsys Prime Time Timing Analyzer
- Typical steps involved in Qualcomm's flow include
 - Placement of inter block logic
 - Top level clock tree synthesis
 - Repeater insertion/optimization for long wires
 - Cross talk analysis and fixes
 - Decoupling capacitor insertion for power jitters
 - Fixes for Electro-migration, manufacturing yield enhancement and process antenna violation
 - Dummy metal insertion to meet minimal metal density of foundry
 - Parasitic extraction
 - Timing, Noise, Power and IR drop analysis
 - Formal Verification using Prime Time Timing Analyzer

Chip Assembly & Signoff

- This is the final step before customer-hand off. The hierarchical GDSII is flattened and final Timing, Noise, IR drop analysis and final physical verification are done. In addition, probe points are inserted.
- STA reports, Physical Verification reports and Tape Out documents are released to customer