

Features

- 3-Bus architecture allows dual operand fetches in every instruction cycle
- Multifunction instructions
- Low power dissipation in idle mode
- ADSP-218x family instruction set compatible
- On-chip RAM of 160K Bytes configured as 32K words on-chip program memory and 32K Words on-chip data memory
- Computational Units
 - Arithmetic Logic Unit
 - Multiplier/Accumulator, and
 - Barrel Shifter
- Two independent data address generators
- Powerful program sequencer provides
 - Zero overhead looping
 - Conditional instruction execution
- Programmable 16-Bit interval timer with prescaler
- Choice of Internal DMA (IDMA) or Byte DMA (BDMA) interface
- 16-Bit Internal DMA port for high speed access to on-chip memory (Mode selectable)
- 8-Bit DMA to 4MB of Byte memory for transparent program and data memory transfers (Mode Selectable).

- 2K I/O Memory interface (Mode Selectable)
- Two double-buffered serial ports with Companding hardware and Automatic data buffering .
- ICE-Port Emulator interface support.
- 100-Lead TQFP package

Functional Overview

VIJAY is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

VIJAY can be used in one of two modes, Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during RESET and cannot be changed while the processor is running.

VIJAY instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle.

The VIJAY contains three independent computational units: ALU, multiplier/accumulator (MAC) and the Barrel Shifter (BS). The computational units process 16-bit data directly and have provisions to support multiprecision

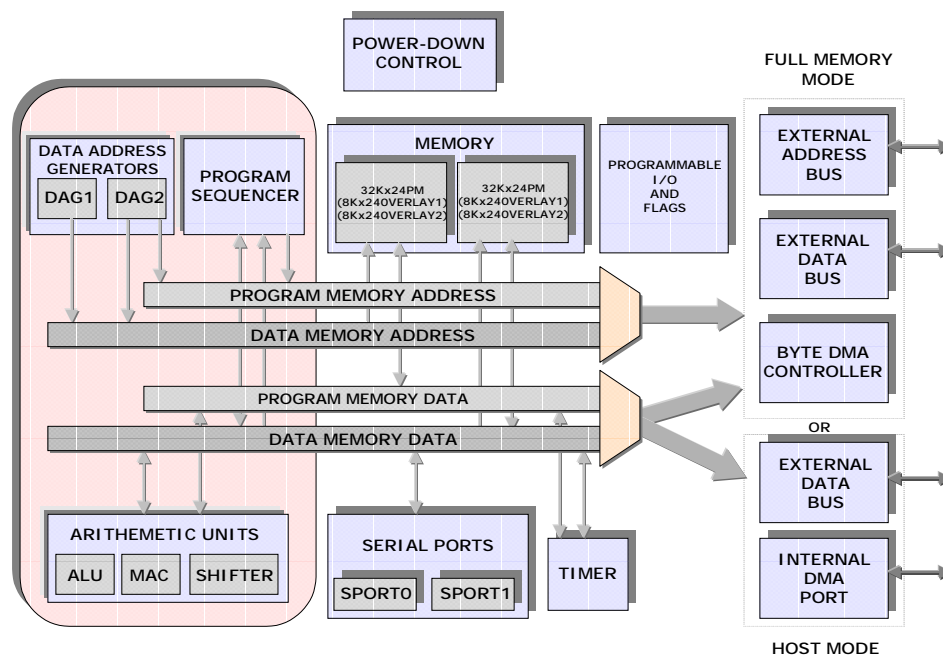
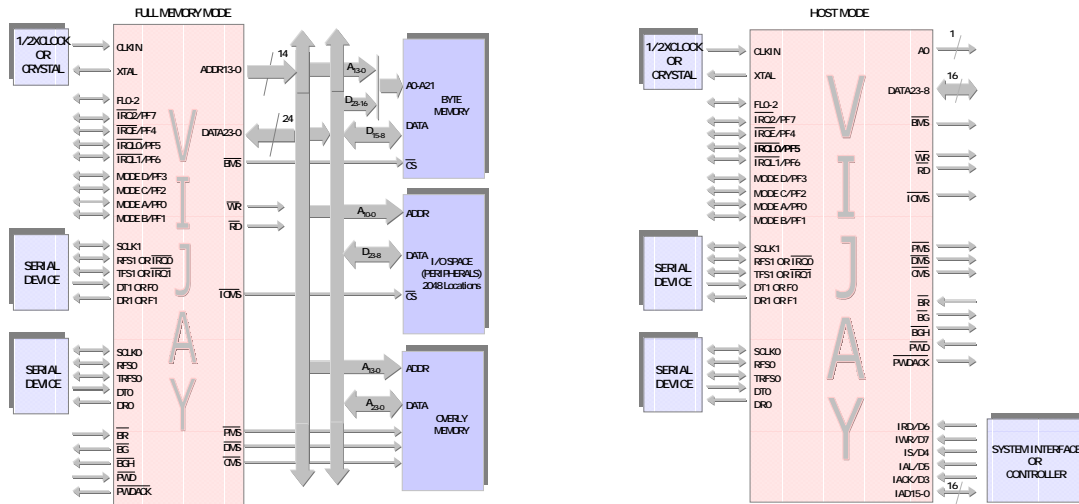


Fig 1: VIJAY Functional Block diagram



computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). DAGs can provide automatic modulo addressing for circular buffers.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port).

VIJAY can respond to eleven interrupts. A programmable interval timer generates periodic interrupts. It provides up to 13 general-purpose flag pins. It incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communication and multiprocessor communication.

Target Applications

- Voice Compression
- Audio Compression
- Spectrum Analysis

Performance

Parameter	Value	Remarks
Gate Count	70K	without memories
Power Estimate		
Code Coverage	87%	97% without MAC
OpenMORE Score		
IP Catalyst Rating		
Technology	0.18 micron	ANAM
Frequency	65	Post-route, worstcase

Deliverables

- Synthesizable verilog RTL code
- Test Bench in verilog
- Synthesis scripts
- User Document
- Verification Document

Additional Items

- Virtual IP Group offers a ready-for-use FPGA based DSP evaluation platform for any customer application. The customer can port their application into the FPGA and can verify it in the evaluation platform

Related Products

- DSP16P, pipe lined architecture
- DSP24P, 24 bit dsp processor

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