V9012P
USB 1.10 Device Core (full-speed)

Features

- **Compliant with USB Specifications Revision 1.10**
- **Supports full-speed (12 Mbps) operation**
- **Supports Remote Wake-up capability**
- **Interfaces with any standard USB transceiver**
- **Interfaces with most of the microcontrollers and microprocessors**
- **Megacell requests to CPU are interrupt driven to minimize the polling time requirements**
- **User friendly Core Generator GUI to choose the required configuration**
- **Configurability to select number of Endpoints as allowed in USB Specification**
- **Configurability to select Endpoint sizes as allowed in USB Specification**
- **Configurability to select single or double buffer for any endpoint**

Functional Overview

V9012P is a USB 1.10 device core that can be readily interfaced with any industry standard microcontroller on one side and with any standard USB transceiver on the other side. The core implements all functionality required at physical (digital) layer and transaction layer of USB specification. The core implements most of the USB protocol related issues in hardware and reduces the load of the microcontroller. Automatic data retry is supported in the core and is not passed on to the higher level software layers. The megacell in a typical USB system is shown in Fig. 1.

The major blocks are the Serial Interface Engine (SIE), Function Interface Unit (FIU), EP Logic and Processor Interface Unit (PIU). SIE block handles NRZI decoding/ encoding, CRC generation/ checking and bit destuffing/ stuffing serial to parallel/ parallel to serial conversion and DPLL logic. EP Logic handles routing of data to/ from the FIFO of the active endpoint. It selects the active endpoint, moves FIFO read/ write pointer to the appropriate location. The number of endpoints and their sizes are configurable through GUI. Each endpoint can be configured to have either single FIFO or double FIFO. The double buffering increases the capacity of the endpoint to handle higher throughput. FIU block provides appropriate handshake response information to SIE. PIU block holds the logic necessary to interface with any generic microcontroller/ processor. The address, data and control signals are synchronized within the core. Megacell provides all signals required to interface with Philips

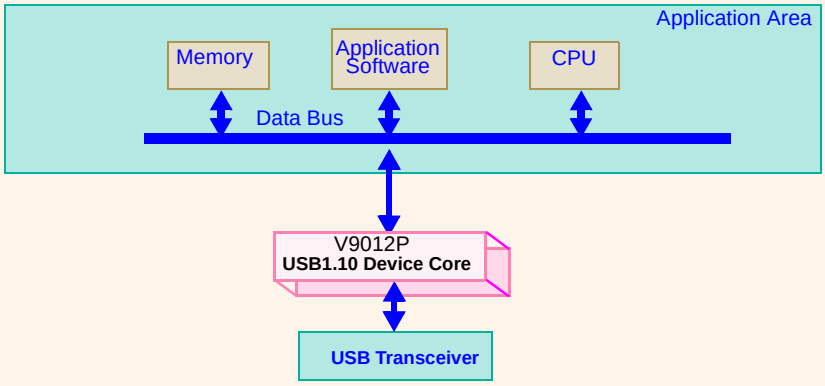

Fig 1: V9012P in a typical USB System

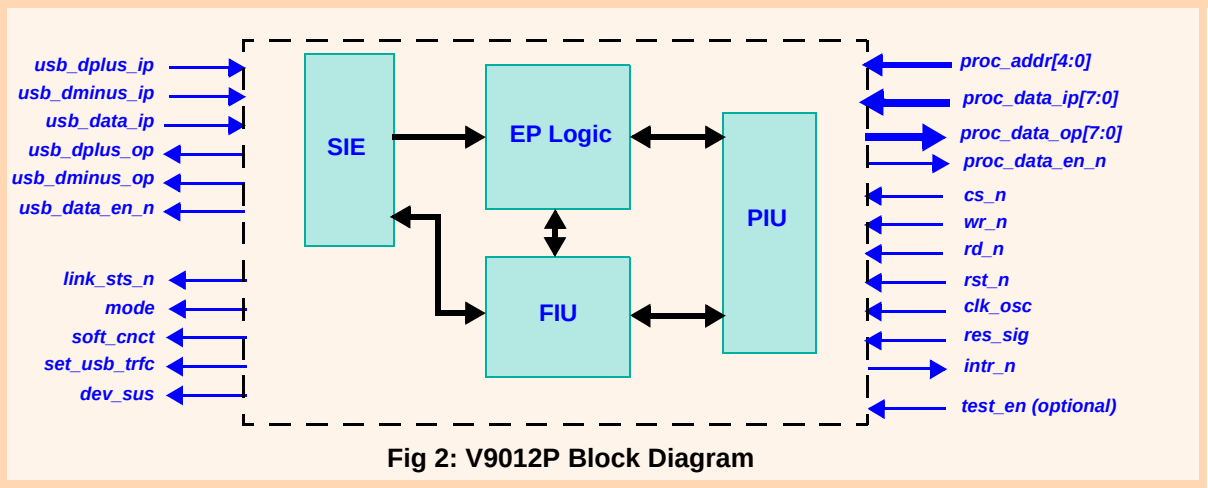

Fig 2: V9012P Block Diagram

PDIUSBP11A transceiver. All signals required to indicate suspend status, resume signal are provided as port level signals. The megacell block diagram is shown in Fig.2.

Performance Specifications

Parameter	Value	Remarks
Gate Count	7K	The gate count excludes FIFO for different endpoints
Power Estimate	-	Not Performed
Code Coverage	99%	Using SureCov tool
OpenMORE Score	95%	As per OpenMORE score sheet
IP Catalyst rating	-	-
Technology	0.25u 0.18u	Avant! passport library Avant! passport library
Frequency	50 MHz	

Target Applications

- This core can be used to develop any USB 1.10 peripheral application
- This core can be used in SoC designs for embedded applications with USB interface

Test Coverage

- Scan insertion is performed using Mentor DFT Advisor
- The ATPG vectors are generated using Mentor Fast Scan and fault coverage of 96% is obtained
- MBIST Architect from Mentor Graphics is used to test the memory

FPGA Evaluation

Application	FPGA	Remarks
18x8 Keyboard	XCV800-6	Interfaced with MCS 51 micro controller and PDIUSBD11A transceiver from Philips
3 button Mouse	XCV800-6	Interfaced with MCS 51 micro-controller and PDIUSBD11A transceiver from Philips
Audio Record-ing and Playback	XCV800-6	Interfaced with ADSP2181 DSP processor and PDIUSBD11A transceiver from Philips

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data sheet, User Guide
- Synthesis Scripts & Timing Constraint files
- Scripts for STA
- Scripts for DFT (Optional)
- Verification Suite

Additional Items

- BIOS calls in C are available to work on 8051 micro-controller. Customers can use BIOS calls to quickly develop applications
- V9012P Reference Design Kit is available as demo as well as a development platform for customers
- USB Client Software Driver development - order based

Related Products

- V9050 USB 2.0 Device Core

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