



# V9201OCP

## Serial ATA Host Controller with OCP Interface

### Features

- Compliant with Serial ATA specification Rev1.0
- Supports Generation 1 serial ATA speed of 1.5Gbps
- Supports a Single Serial ATA PHY interface conforming to SAPIs Draft Rev 0.90
- CONT primitive transmission support for continued primitive suppression
- Support for first party DMA transfers
- Supports slumber and partial power down modes
- Low frequency operation (37.5 Mhz) in Link and Transport layers for generation1 speed
- 256 Byte FIFO Implemented with RAMs in Transmit and Receive paths
- Supports PHY interface widths of 10bit, 20bit and 40bit
- Configuration through a basic OCP interface
- Programmable Interrupt sources to attract CPU attention
- Inbuilt DMA controller to perform Bus Master DMA operations
- DMA Data Transfers through a simple extension OCP bus
- PIO Data Transfers through Basic OCP bus
- Configurable data and configuration OCP bus widths of 16, 32 and 64 bits
- Reuse of the core across different On-Chip Buses with the help of standard Bus Wrappers

### Functional Overview

SATA specification defines four layers namely Physical layer, Link Layer, Transport Layer and Application Layer. Physical layer performs serialization/deserialization of data, extraction of clock, power on sequencing and Out Of Band signalling transmission and reception.

Link layer basically performs frame transmission and reception. It inserts SOF, EOF, CRC (mandatory) and other primitives (if required) within the data given by the transport layer, performs 8b/10b encoding and 10b/8b decoding, scrambles the data in such a way to distribute the potential EMI emissions over a broad range and reports status of frame transmission/reception to transport layer.

Transport layer basically performs FIS construction and FIS decomposition. It also notifies the link layer of the required data flow control, reports the transmission/reception status to the application layer.

The Application layer has the software control, Buffer memory and DMA engines.

The SATA Host Controller implements the Link layer, transport layer and some part of the application layer. In the receive direction, SATA Host controller takes the parallel data from the PHY and slips the ALIGN sequences and passes a dword to the link layer block. The link layer performs 8b/10b decoding, primitive detection and

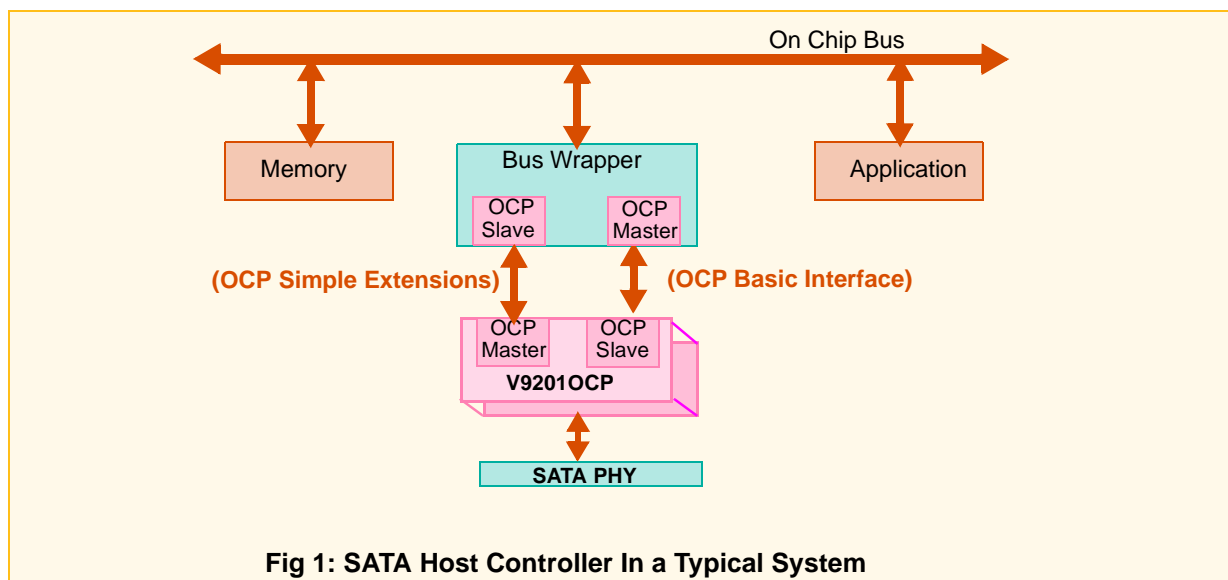
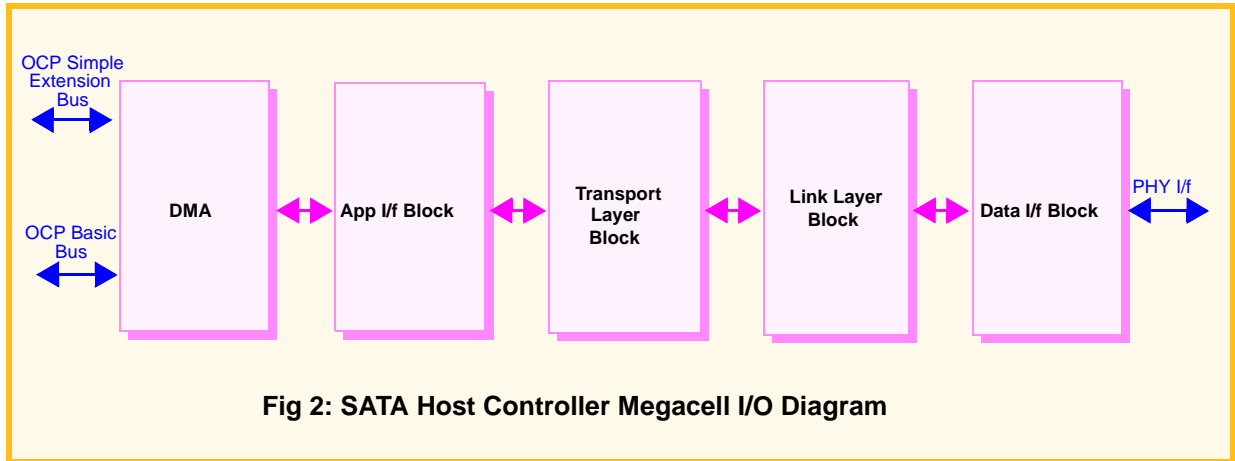


Fig 1: SATA Host Controller In a Typical System



**Fig 2: SATA Host Controller Megacell I/O Diagram**

descrambling and CRC checking. A state machine in the link layer manages the data transfers between the peer and the host. The data is then delivered to the transport block where FIS type detection and decomposition is done. The data is then given to the application layer block where it is stored in the FIFO or loaded into the registers depending upon the FIS type. The data in the FIFO is then transferred through DMA or PIO transfer when the threshold is reached. The link layer block performs the necessary flow control depending upon the FIFO status signals.

In the transmit direction, data is filled in the FIFO through DMA transfer or PIO transfer and DATA FIS transmission is initiated by the transport layer block. The link layer block performs CRC calculation on this data along with scrambling and 8b/10b encoding. The link layer state machine performs the flow control when the PIO transfer or DMA fails to catch up with the SATA data transfer rate.

environment

- This Core can be easily interfaced with any OCP master core to develop SATA Host functionality
- Any application where in a SATA device like hard disk, CDROM etc. needs to be connected to a Host

### Test Coverage

- Design is highly synchronous and scan friendly
- Fault coverage is 97% with ATPG vectors

### Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite
- Synthesis Scripts
- Scripts for STA & DFT (optional)

### Performance

Parameter	Value	Remarks
Gate Count	60k	For 32bit OCP bus and 10 bit PHY i/f (excluding RAM)
Code Coverage	98%	Block, Arc, State Transitions, Expressions, Events
OpenMORE Score	91%	
Technology	0.18	TSMC, Artisan
Frequency	60 -160 MHz	STA verified on pre-route, post-scan netlist

### Target Applications

- This Core is intended for use in SoC designs due to the flexibility it offers to get easily integrated in to any SoC

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