



# V6210

## PCI-Express Initiator/Target Endpoint Controller

### Features

- Complies with PCI-Express Base Specification Rev1.0a
- Phy Interface complies with Intel PIPE spec Rev 1.0
- Fully compliant with PCI Express transaction ordering rules
- Configurable Tx, Rx and Retry buffer sizes
- Configurable Max payload size (128 bytes to 4k bytes)
- Flexible Back-end Application Interface
  - 64/32 bit, Application Data bus width
  - User choice of Application interface clock rate
- Type 0 Configuration Space Header
- Upto 6 configurable Base Address Registers (Memory or I/O)
- Expansion ROM Base Address Register
- Supports Power Management Interface (PMI) and Active State Power Management
- Supports Message Signalled Interrupt (MSI)
- Implements the optional features like:
  - Advanced Error Capability structure
  - VC Capacity structure
  - End-to-End CRC
- Supports Remote Loopback as a Slave, also supports for Phy local Loopback
- Supports Hot-Plug and Hot-Removal
- Supports x1, x2, x4 and x8 lanes<sup>1</sup>
- Supports upto 8 Virtual Channels<sup>2</sup>

**Note:** 1. Only x1 lane is supported in the initial release  
2. Only Two VCs are supported in the initial release

### Functional Overview

The V6210 is a high-performance, technology independent, synthesizable core that implements the PCI-Express Base Spec Rev1.0a for PCI-Express initiator and target endpoint applications. The core supports a wide variety of design implementations and features an easy-to-use application interface. The general use of the core in a system is shown in Fig 1: V6210 Megacell in a Typical Application.

The V6210 core acts as a requester and completer. The PCI express is a layered architecture and is defined as transaction layer, data link layer and physical layer. Each layer is divided into TX and RX channels as shown in Fig 2: V6210 Megacell Functional Block Diagram. Configuration and Power management block contains all the configuration registers and power management control logic.

### Transaction Layer

The transaction layer is an upper layer of the PCI-Express core architecture. The main function of this layer is assembly and disassembly of Transaction Layer Packets (TLPs). This layer is also responsible for the transaction ordering, TC to VC mapping and credit based flow control management.

The TX section accepts the requests from the application interface and constructs the TLP and forwards it to data link layer. The RX section receives the TLPs from data link layer and checks against the TLP formation rules and forwards to application interface.

### Data Link Layer

The data link layer is an intermediate stage between the Transaction Layer and the Physical Layer. This layer is responsible for the link management, data integrity and flow control initialization.

The TX section accepts the TLPs from the Transaction layer and it adds a TLP sequence number in the beginning of the packet and appends the LCRC at the end of the packet. It also generates and transmits DLLPs for ACK/NAK protocol, Flow control and Power Management functions. The RX section receives TLPs from the MAC layer and checks for LCRC and forwards it to Transaction layer.

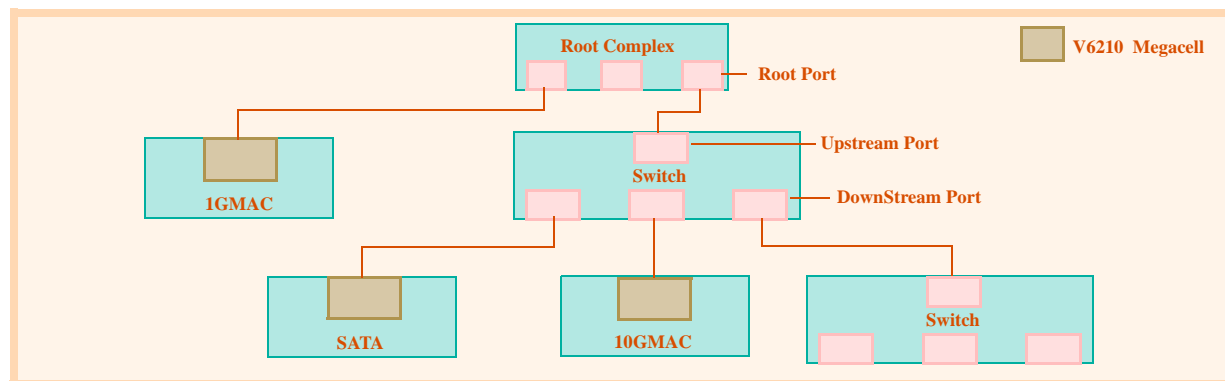
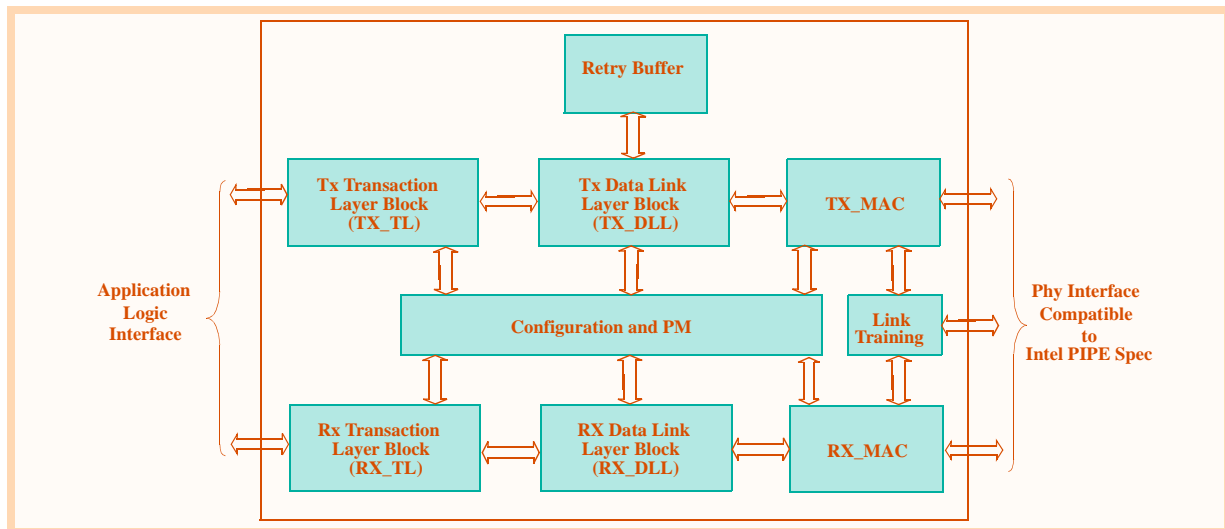


Fig 1: V6210 Megacell in a Typical Application



**Fig 2: V6210 Megacell Functional Block Diagram**

### Phy MAC Layer

Phy MAC layer is the lower layer of the PCI-Express core architecture. The Phy interface complies with the Intel's PIPE spec Rev1.0.

The LTSSM block is responsible for Link negotiation. The TX MAC block accepts the TLP/DLLP from Data link layer and forwards it onto the Phy interface after scrambling. It also adds a STP/SDP symbol at the beginning of the packet and appends END/EDB symbol at the end of the packet. This block also schedules and transmits different types of Ordered Sets depending upon the state of LTSSM. The RX MAC block receives packets from the Phy interface and forwards them to the Data link layer after de-scrambling.

### Configuration & PM

The Configuration and Power Management block implements the PCI type zero header, MSI and PM capability structures. It also implements the optional VC capability structure, Advanced Error management structure. This block also implements the logic required for sending error messages and for Active State Power Management.

### Performance Specifications

Parameter	Value	Remarks
Code Coverage	100%	
OpenMORE Score	96%	
Technology	0.13u	Artisan TSMC, CSM
Frequency	125MHz	

### Target Applications

- Telecommunication Networks
- High performance I/O applications like 10GMAC, SATA etc.,
- High bandwidth Digital Video applications

- To develop independent PCI-Express based applications
- In SoC designs requiring PCI-Express interface

### Deliverables

- Fully synthesizable Verilog RTL Source code
- Documentation - Data sheet, User Guide
- Synthesis Scripts
- Scripts for STA & DFT (optional)

### Related Products

- V6202 PCI-2.2 Initiator/Target Core
- V6201 PCI-X Initiator/Target Core