V6202
PCI-2.2 Initiator/Target Core

Features

- **PCI Revision 2.2 compliant**
- **Supports 33/66MHz PCI-2.2 Bus**
- **Supports PCI 2.2 functions**
  - 64/32 bit, PCI-2.2 initiator and target Interface
  - 64-bit Addressing support (DAC)
  - I/O Read, I/O Write, Configuration Read and Configuration Write, Special Cycles, Interrupt acknowledge cycles
  - Memory Read, Memory Read Multiple, Memory Read Line
  - Memory Write, Memory Write and Invalidate
  - Type 0 Configuration Space Header
  - Upto 6 Base Address Registers (Memory or I/O)
  - Expansion ROM Base Address Register
  - Cardbus CIS pointer Address Register
  - Parity generation, Parity Error Detection, Target Abort, Target Retry, Target Disconnect, Master Abort
  - Full Command and Status Registers
  - Supports fast back-to-back transactions as a target
  - Supports exclusive lock transactions
- **Supports Fully Synchronous Application interface**
  - Separate paths for Initiator Receive and Transmit
  - Separate Paths for Target Receive and Transmit
- **Configurable features**
  - 64/32 bit AD bus width
  - DAC support in initiator
  - Selectable Configuration space registers and values
  - Power Management Interface (PMI)
  - VPD Support
  - Message Signalled Interrupts (MSI)

Functional Overview

The V6202 is a high-performance, technology independent, synthesizable core that implements the PCI-2.2 Local Bus protocol for PCI initiator and target applications. The core supports a wide variety of design implementations and features an easy-to-use application interface. The general use of the core in a system is shown in Fig 1: V6202 Megacell in a Typical Application

The V6202 Megacell supports fully compliant burst operations for both sourcing data and receiving data. Transfer rates of up to 528 MB per second are achievable on a 64-bit, 66 MHz PCI-2.2 bus. This core is partitioned into 4 major blocks Data path, PCIbus_mux, Configuration space, Target and Initiator as shown in Fig 2: V6202 Megacell I/O Diagram.

The PCIbus_mux block multiplexes the initiator and target address/data buses and control signals. It contains four data paths in and out for both target and Initiator. The four unidirectional paths are multiplexed inside the core. All the data transfers are register-to-register. Since there are only a few registers on each data path, loading is reduced and false timing paths are eliminated.

The Configuration Space block holds type 0 configuration space header in the first 64-bytes, next 64-bytes are reserved for extended capabilities and remaining 128-bytes are available for user application.

The Target and Initiator blocks provides a simplified, synchronous target and initiator interface. The PCI bus width is configurable to 32 or 64 bit. The core automatically handles conversion of 32/64 bit regardless of the PCI bus width.

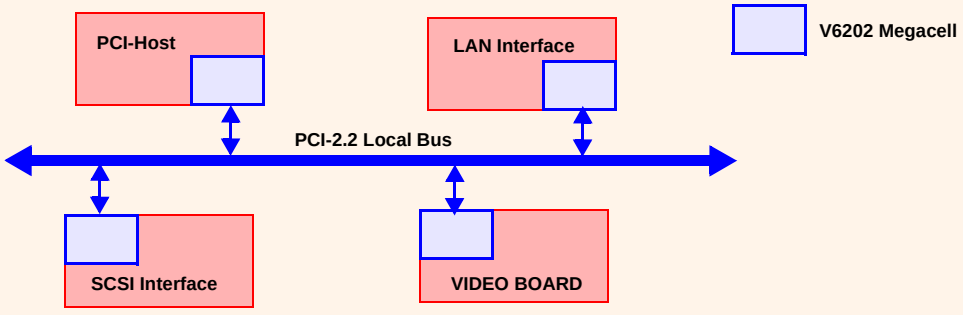

Fig 1: V6202 Megacell in a Typical Application

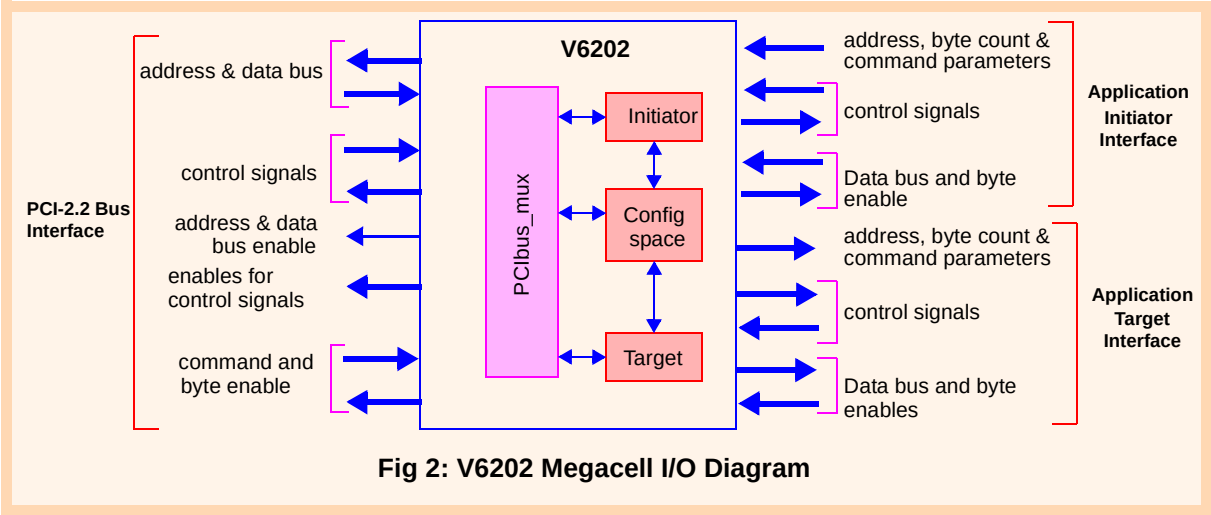

Fig 2: V6202 Megacell I/O Diagram

Performance Specifications

Parameter	Value	Remarks
Gate Count	~27K ~19K	64-Bit (excluding pads) 32-bit (excluding pads)
Code Coverage	100%	Block, Arc, State Transitions, Expressions, Events
OpenMORE Score	96%	
Technology	0.18u	Artisan, TSMC
Frequency	66MHz	STA verified on pre-route, post-scan netlist

Target Applications

- Embedded applications in networking requiring PCI-2.2 interface
- High performance I/O applications requiring faster data transfers
- To develop independent PCI-2.2 based application
- In SoC designs requiring PCI 2.2 interface

Test Coverage

- Design is highly synchronous and scan friendly
- Fault coverage is 98% with ATPG vectors

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite
- Synthesis Scripts
- Scripts for STA & DFT (optional)

Related Products

- V6201 PCI-X Initiator/Target Core

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