V6301OCP
Parallel ATA Controller with OCP Interface

Features

- **Compliant to ATA/ATAPI -6 interface format definition**
- **Programmability to hold the configuration bus till the requested transaction completed in case of PIO transfers and for Task file register access**
- **Programmable PIO transfer timings for Mode0 to Mode4**
- **Programmable multiword DMA transfer timings for Mode0 to Mode2**
- **Programmable Ultra DMA timings for Mode0 to Mode5**
- **Provides synchronous interface on the device side**
- **Configurable FIFO depth to achieve required DMA transfer rates**
- **Configurability of OCP interface bus width to 16/32/64**
- **Reuse of the core across different On Chip Buses with the help of standard Bus Wrappers**

Functional Overview

V6301OCP is a ATA/ATAPI host controller. The V6301OCP handles PIO, Multiword DMA (MDMA) and Ultra DMA (UDMA) data transfers with ATA/ATAPI compliant device. OCP interface is provided on the Host side. The OCP interface makes the core independent of the SOC bus and increases the reuse across different embedded applications. A CPU Host can control and monitor the V6301OCP through a set of configuration and control registers. Transfers can be carried out through either PIO modes,Multiword DMA modes or Ultra DMA modes. And each of above modes can be progammed via timing registers.

The major blocks of V6301OCP are

DMA Controller to carry the transfers from PATA Controller to system memory and vice-versa.

PIO Engine in which PIO and Register transfer protocol are implemented.

MDMA Engine in which Multiword DMA protocol is implemented.

UDMA Engine in which Ultra DMA protocol is implemented.

FIFO control block, in which FIFO pointer logic, read unpack and write pack logic are implemented.

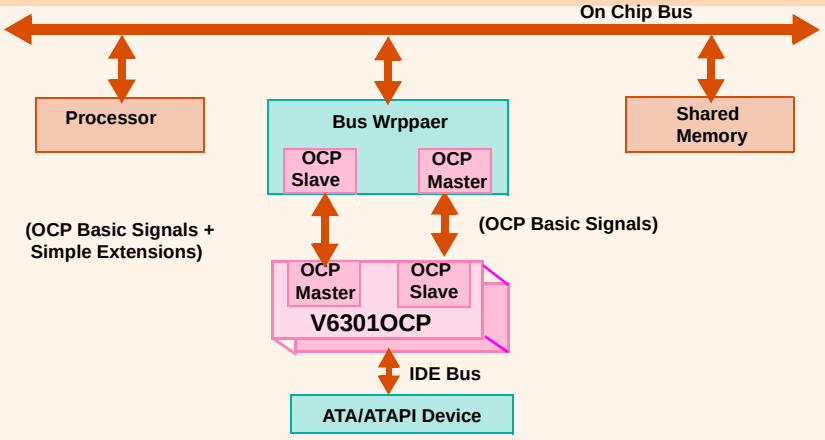

Fig 1: V6301OCP in a Typical System

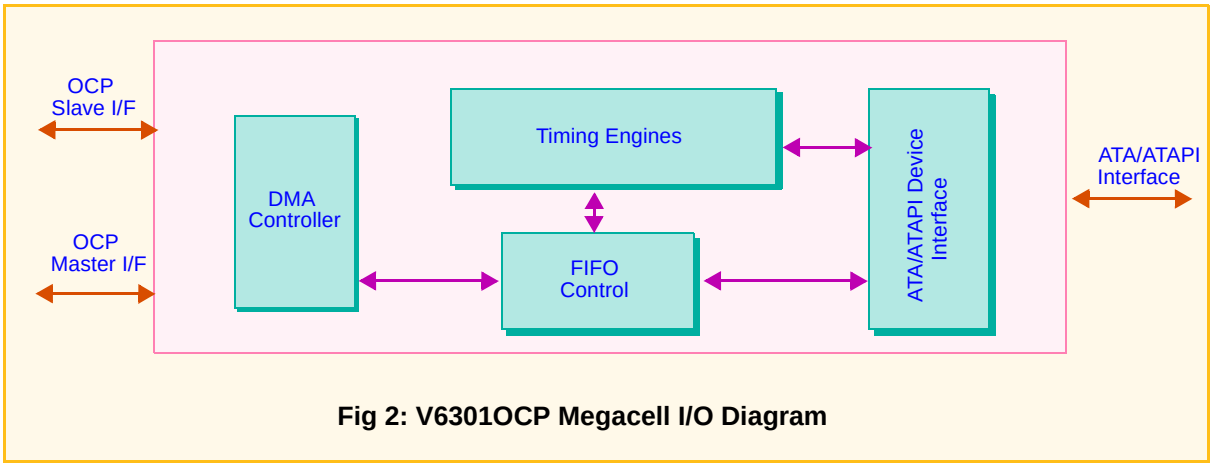

Fig 2: V6301OCP Megacell I/O Diagram

Performance Specifications

Parameter	Value	Remarks
Gate Count	~25K	includes DMA and excluding RAM
Code Coverage	100%	Block, Arc, State Transitions, Expressions, Events
OpenMORE Score	96%	
Technology	0.18µ	Artisan, TSMC
Frequency	40 - 160 MHz	STA verified on pre-route netlist

Target Applications

- This Core is intended for use in SoC designs due to the flexibility it offers for easy integration in to any SoC environment
- This Core can be easily interfaced with any OCP compliant cores to develop wide variety of Parallel ATA peripheral applications

Test Coverage

- Design is highly synchronous and DFT friendly
- Fault coverage is 96% with ATPG vectors

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite
- Synthesis Scripts
- Scripts for STA & DFT (optional)

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