V9401OCP
I2C Controller with OCP Interface

Features

- **Supports bi-directional transfer**
- **Master support for both transmit and receive**
- **Supports standard, fast and high speed modes**
- **Supports both 7-bit and 10-bit addressing**
- **START, STOP, and REPEATED START condition generation**
- **Programmable fast or standard mode**
- **Supports automatic switching to high speed mode**
- **Start Byte feature**
- **General Call address feature**
- **Application interface fully complies with OCP slave specification (basic)**
- **Configurable OCP databus width to 16/32/64 bits**
- **Reuse of the core across different On Chip Buses with the help of standard OCP Bus Wrappers**

Functional Overview

The Inter-IC (I2C) bus is a 2-wire synchronous, multi-master, bi-directional bus interface that provides a simple and efficient way to exchange data among any type of integrated circuit devices such as mircocontrollers, EEPROMs, real-time clock devices, A/D converters and LCDs. The multi-master support allows the connection of additional devices to the bus for expansion and system development.

The V9401 core acts as an I2C bus master. Master can initiate the transaction either for reading data from slave or writing data to slave. V9401 interfaces on one side with I2C bus and on the other side with OCP compliant basic interface. The OCP socket interface makes the core independent of the SoC bus and increases its reuse across different applications by using standard bus wrapper. The two-wire bus minimizes device interconnections. The usage of the core in a system is shown in Fig 1: V9401OCP in a Typical Application.

The serial side interface supports 100kHz/400kHz/ 3.14MHz for various applications. All operations of the core can be controlled and monitored through a set of control and status registers.

The major blocks of the design are serial clock generator, transmitter, receiver and registers. The serial clock generator drives serial clock line. The transmitter and receiver control the data flow by holding the clock line whenever device is not ready. They generate an interrupt to the CPU in application area after a byte of data trans-

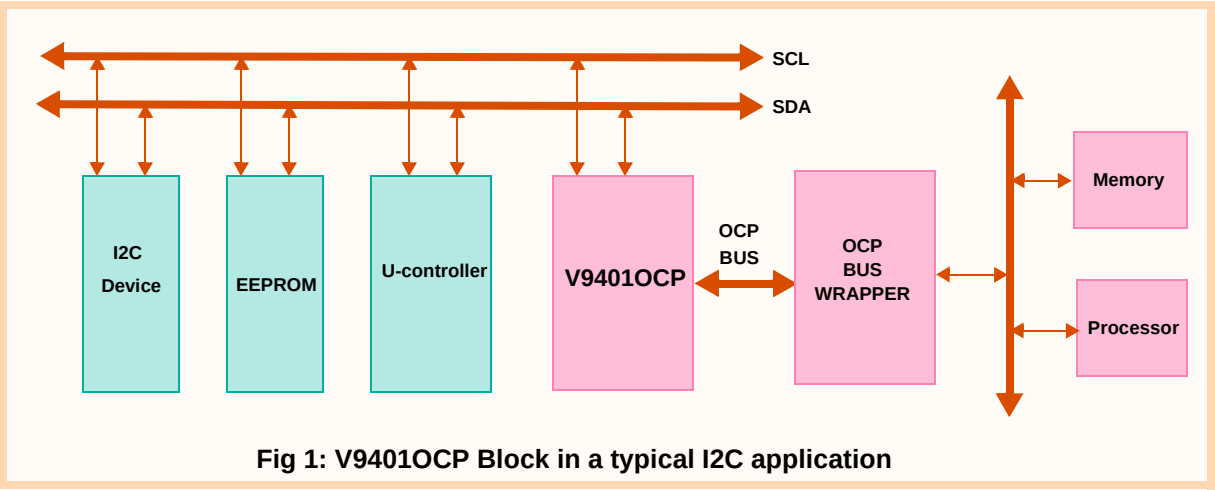

Fig 1: V9401OCP Block in a typical I2C application

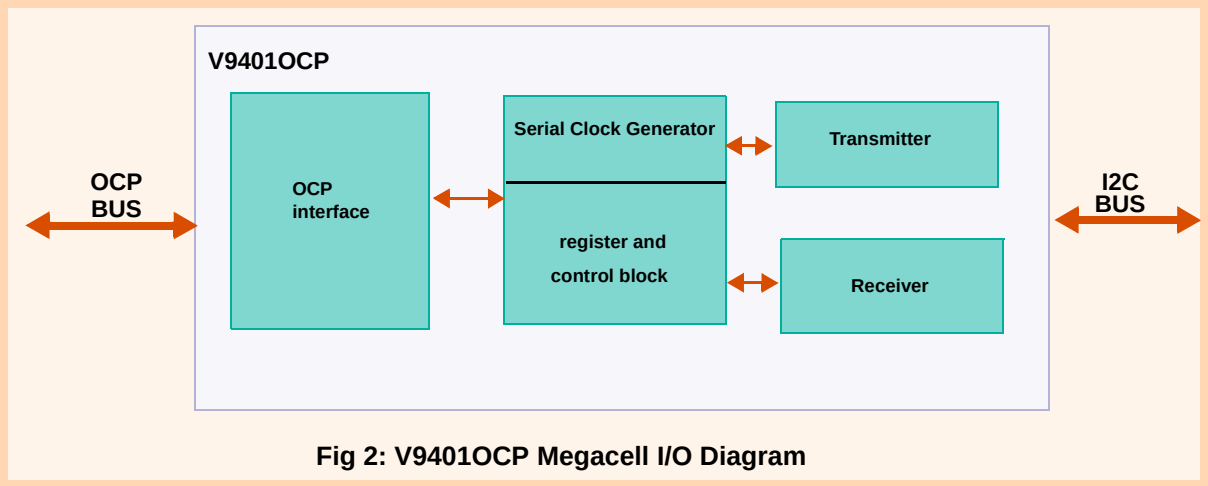

Fig 2: V9401OCP Megacell I/O Diagram

ferred or received. The design provides interrupt as an OCP sideband signal. The I/O details of the core are shown in Fig 2: V9401OCP Megacell I/O Diagram.

Performance Specifications

Parameter	Value	Remarks
Gate Count	1.7K	32-bit config bus
Code Coverage	100%	Block, Arc, State Transitions, Expressions, Events
OpenMORE Score	96%	
Technology	0.18u	Artisan, TSMC
Frequency	175 MHz	STA verified on post scan netlist

Target Applications

- Exchange data with other I2C devices such as mirco-controllers, EEPROMs, real-time clock devices, A/D converters, and LCDs.
- Power On SoC Configuration from EEPROM
- In any SoC design with requirement to integrate I2C controller

Test Coverage

- Design is highly synchronous and scan friendly
- Fault coverage is 99% with ATPG vectors

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite
- Synthesis Scripts
- Scripts for STA & DFT (optional)

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