

STANDARD CELL LIBRARY DESIGN

... NEW BUSINESS WING

Standard Cell library

1. Standard cell libraries are required by almost all CAD tools for chip design.
2. Standard cell libraries contain primitive cells required for digital design. However, more complex cells that have been specially optimized can also be included.
3. The final output from the design process is in the GDSII (gds2) format.
4. To produce a functionally correct design that meets all the specifications and Constraints, requires a combination of different tools in the design flows.
5. These tools require specific information in different formats for each of the cells in the standard cell library provided to them for the design.

Standard Cell library

The formats explained here are for Cadence tools, however similar information is required for other tool suites.

1. Physical Layout (gdsII, Virtuoso Layout Editor) Should follow specific design standards eg. constant height, offsets etc.
2. Logical View (verilog description or TLF). Verilog is required for dynamic simulation. Place and route tools usually can use TLF. Verilog description should preferably support back annotation of timing information.
3. Abstract View (Cadence Abstract Generator, LEF). LEF: Contains information about each cell as well as technology information

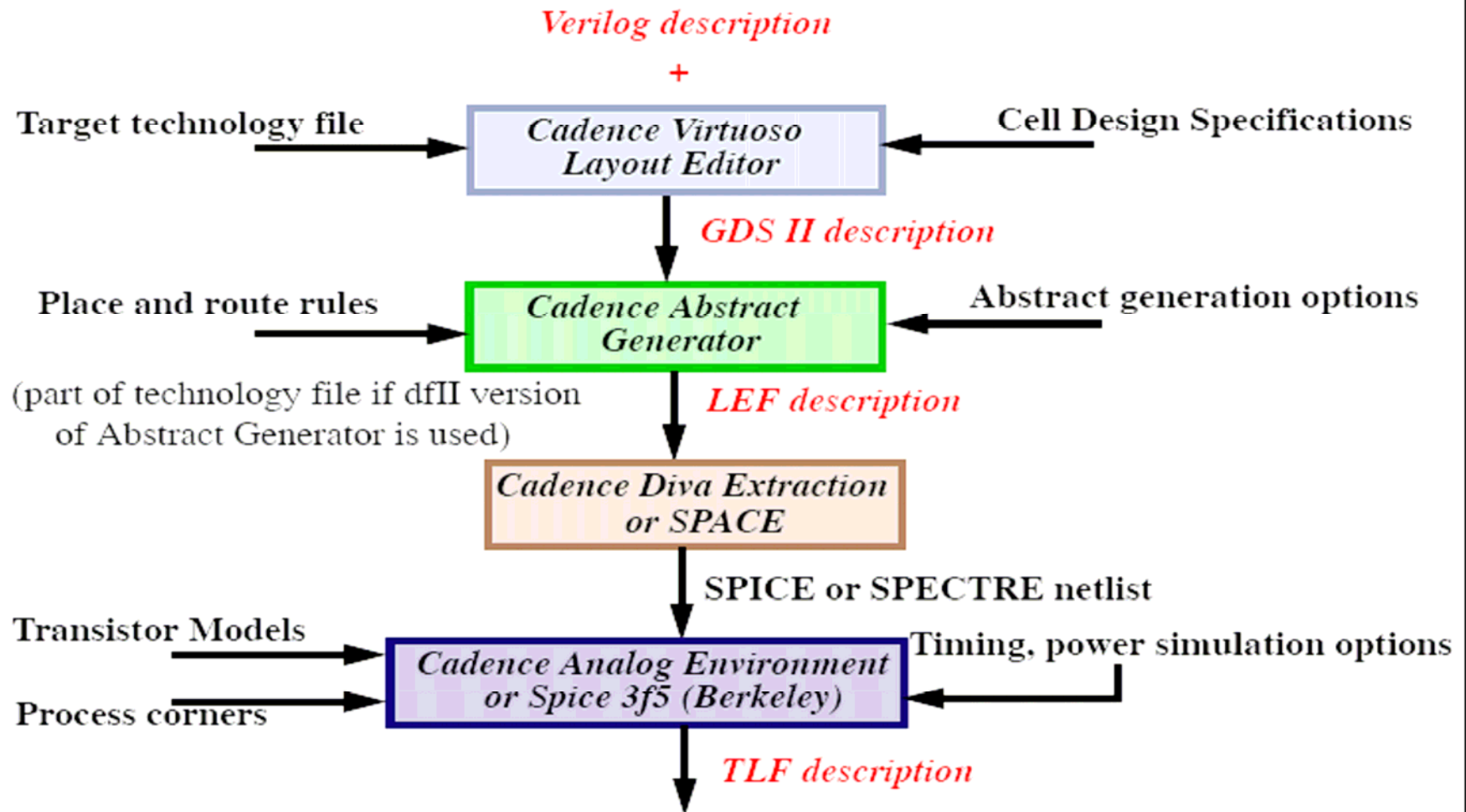
4. Timing, power and parasitics (TLF). Transistor and interconnect parasitics are extracted using Cadence. Spice or Spectre netlist is generated and detailed timing simulations are performed.

Power information can also be generated during these simulations. Data is formatted into a TLF file including process, temperature and supply voltage variations.

Logical information for each cell is also contained in the TLF file.

Standard QCL Flow

Standard Cell Library Formats



Inputs Required From the customer

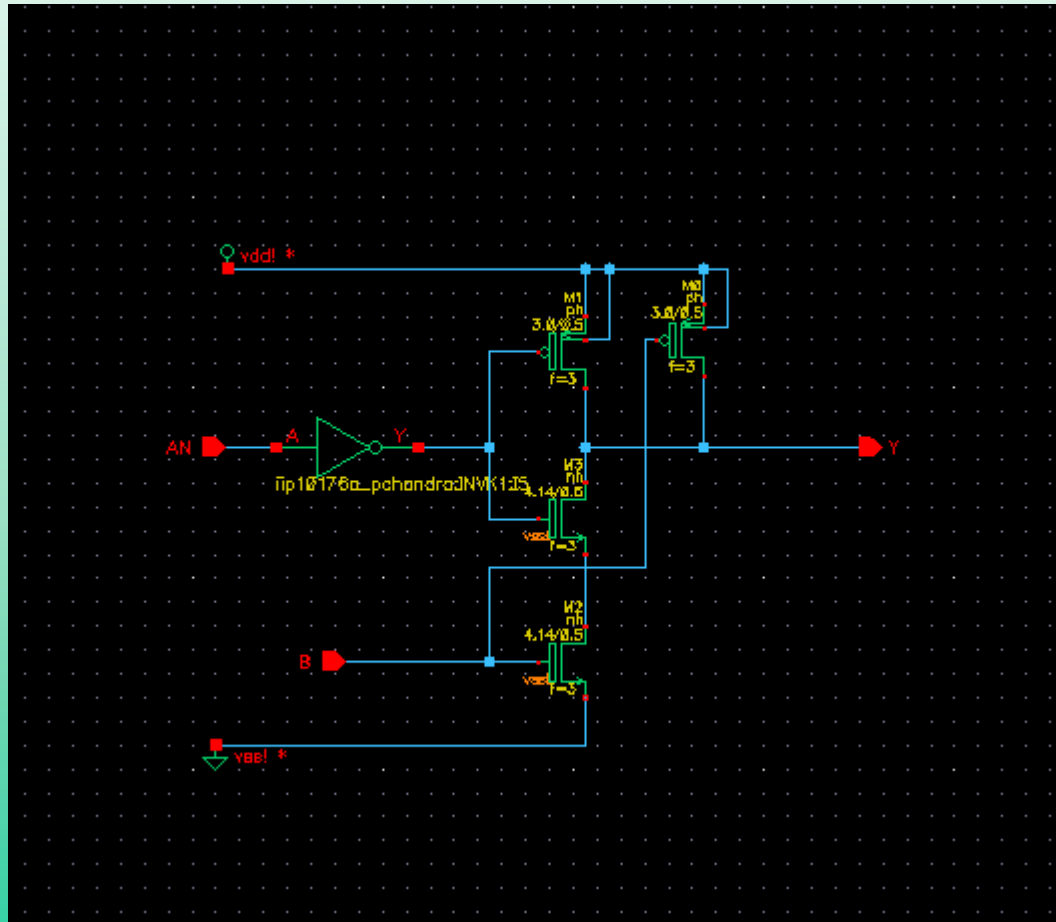
1. Standard Cell Height
2. Horizontal Pitch
3. Vertical Pitch
4. Horizontal Offset
5. Vertical Offset
4. VDD/VSS Power Metal Width
5. No of Metals up to which we can use in the Std cell level

Layout rules

1. All Cells Should be of Same Height which is Decided by the Customer.
2. All standard cells Width Should be Multiples of Horizontal grid.
3. Make sure that the Std cell height is Sufficient for Complex cells in order to avoid Multiple fingers so that routing complexity is going to be reduced.
4. Try to minimize poly routing as the poly has high sheet resistance which introduces parasitic capacitance and resistance.
5. Try to put more contacts in VDD/VSS Rails so that it is going to reduce the contact resistance of power rails.

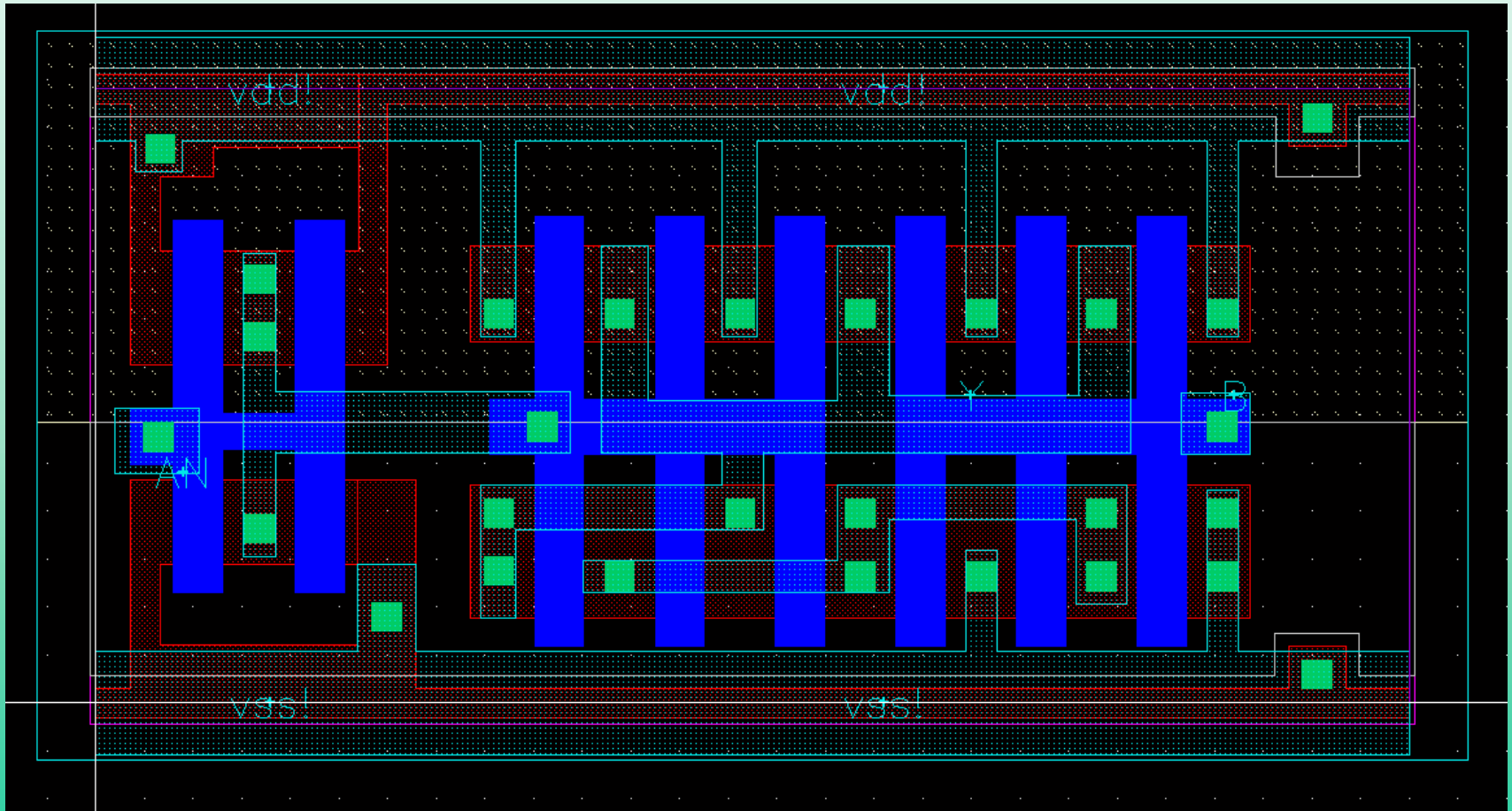
6. At least one substrate contact should be placed in VSS bus in order to Avoid latch up.
7. Make sure that Antenna deck is included in the DRC Deck otherwise we need to Clean Antenna Violations also.
8. Metals which are connected to Pins should be stretched to intersection of Horizontal and vertical offsets.
9. Always follow Minimum DRC rules.

Sample cells –schematic view



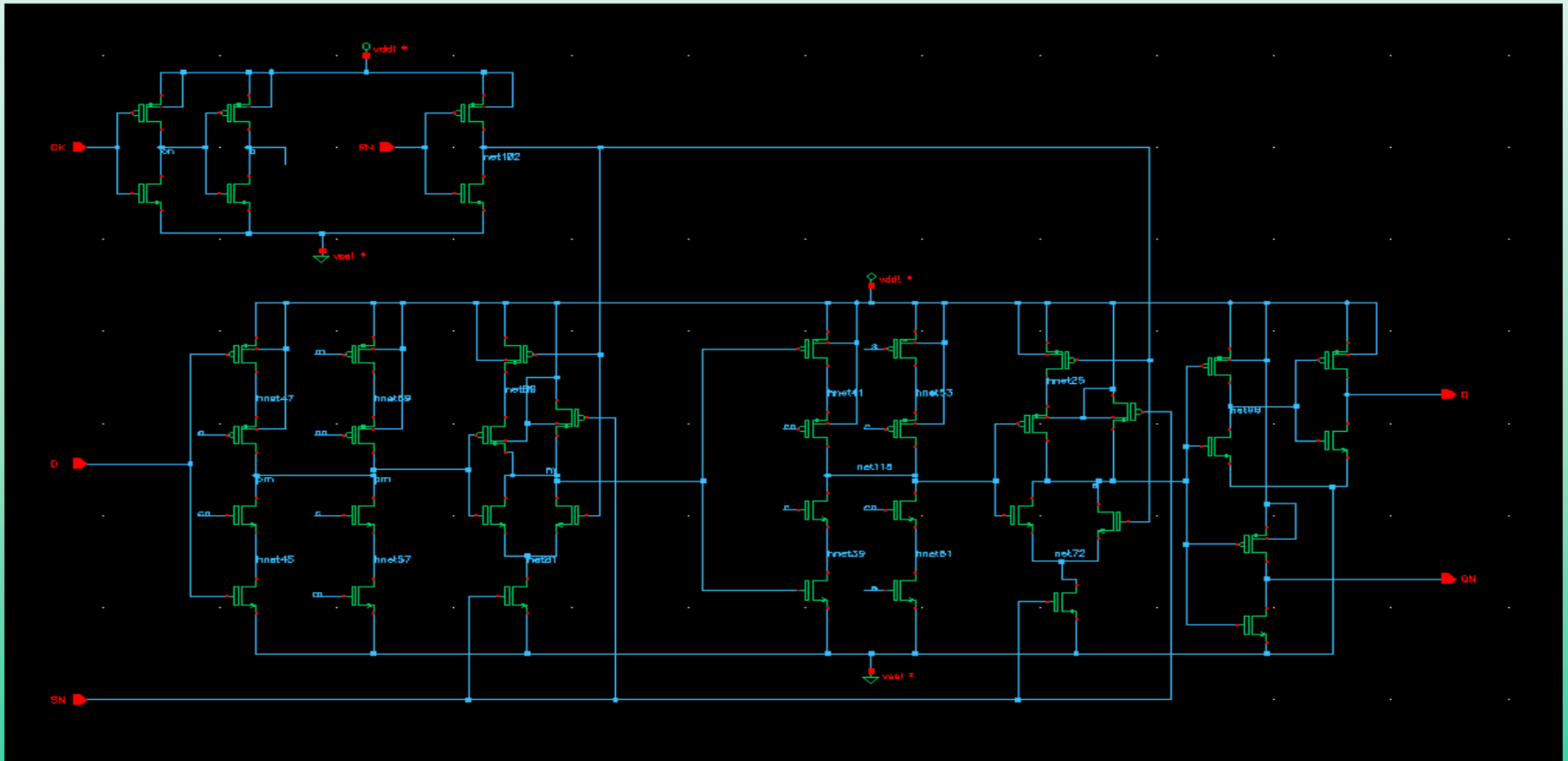
Input bubbled NAND-Schematic view

Sample cells –layout view



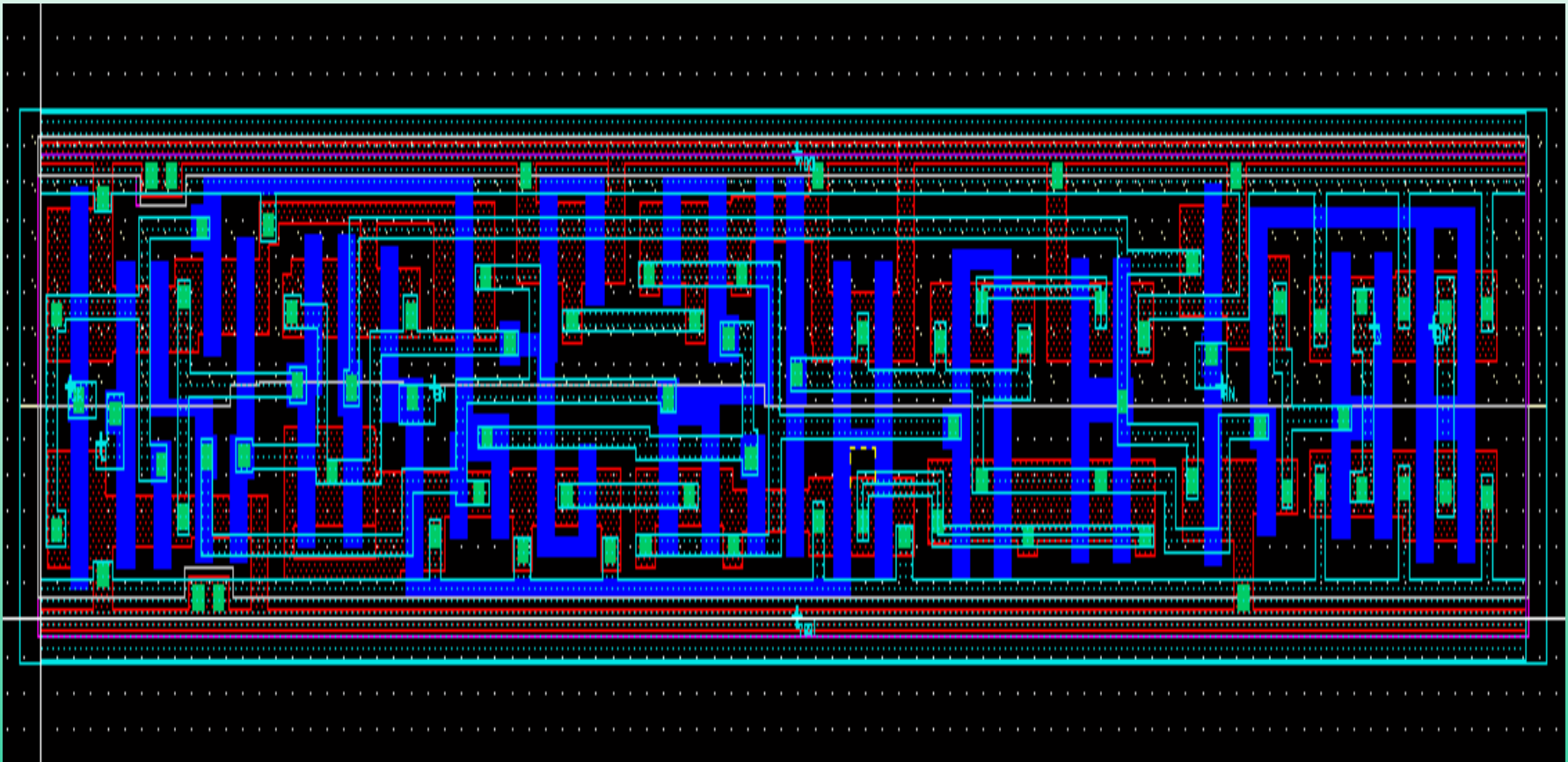
Input bubbled NAND –Layout view

Sample cells –schematic view



D flip-flop –Schematic view

Sample cells –layout view



D Flip flop –Layout view

Thanks