

QCUSB1-09T

Hi-Speed USB Host, Device or OTG PHY with UTMI+ Level 3 Interface



General Description

The QCUSB1-09T is a transceiver that complies with the physical layer specification of USB Revision 2.0. The QCUSB1-09T Hi-Speed USB PHY operates as Device, Host or OTG with UTMI+ Level3 Interface. Internal pull-up and series resistors are incorporated into the I/O and connected to the DP and DM pads. It incorporates clock and data recovery circuitry. The PHY supports 16-bit bi-directional, 16-bit unidirectional interface, 8-bit bi-directional interface and 8-bit unidirectional interface.

During TRANSMIT mode, the QCUSB1-09T serializes data and generates SYNC and EOP fields. It also provides stuffing and encoding using NRZI technique. During RECEIVE mode, the QCUSB1-09T de-serializes incoming data, removing SYNC and EOP fields. It also performs bit un-stuffing and NRZI decoding. The QCUSB1-09T Transceiver I/O is implemented in 1P9M 90nm CMOS Logic process.

Applications

Printers/Scanners
PDAs
Mobile Phones, Wireless Internet
Digital Cameras & Printing Photos
CD-RW
Gaming Devices

Features

- Designed for TSMC CLN90GOD & CLN90G Low K, 90nm, 1P9M, 1.0V/3.3V CMOS logic process
- Cell uses 1P9M
- Size – 1225um x 800um
- Ports on M3-M8
- Compliant to USB Specification Rev. 2.0
- Interface compliant with UTMI+ Level3 specification Revision 1.0
- Includes full support for the optional On-The-Go specification
- Supports high speed (480 Mb/s), full speed (12Mb/s) and low speed (1.5 Mb/s) operation
- Sync and EOP generation on transmitting packets and detection on receive packets
- NRZI Encoding/Decoding
- Bit stuffing and bit un-stuffing with error detection
- Support for all test modes as defined in USB2.0 specification
- Supports the suspend state, HS detection, HS chirp, Reset and Resume operations.
- Ability to switch between FS and HS terminations/signaling
- Integrated 45 ohm termination resistors, 1.5K Ω pull-up resistor and 15K Ω pull-down resistor
- Incorporates crossing voltage control circuit
- Pads incorporate ESD structures
- Antenna diodes on all digital core pins

QCUSB1-09T

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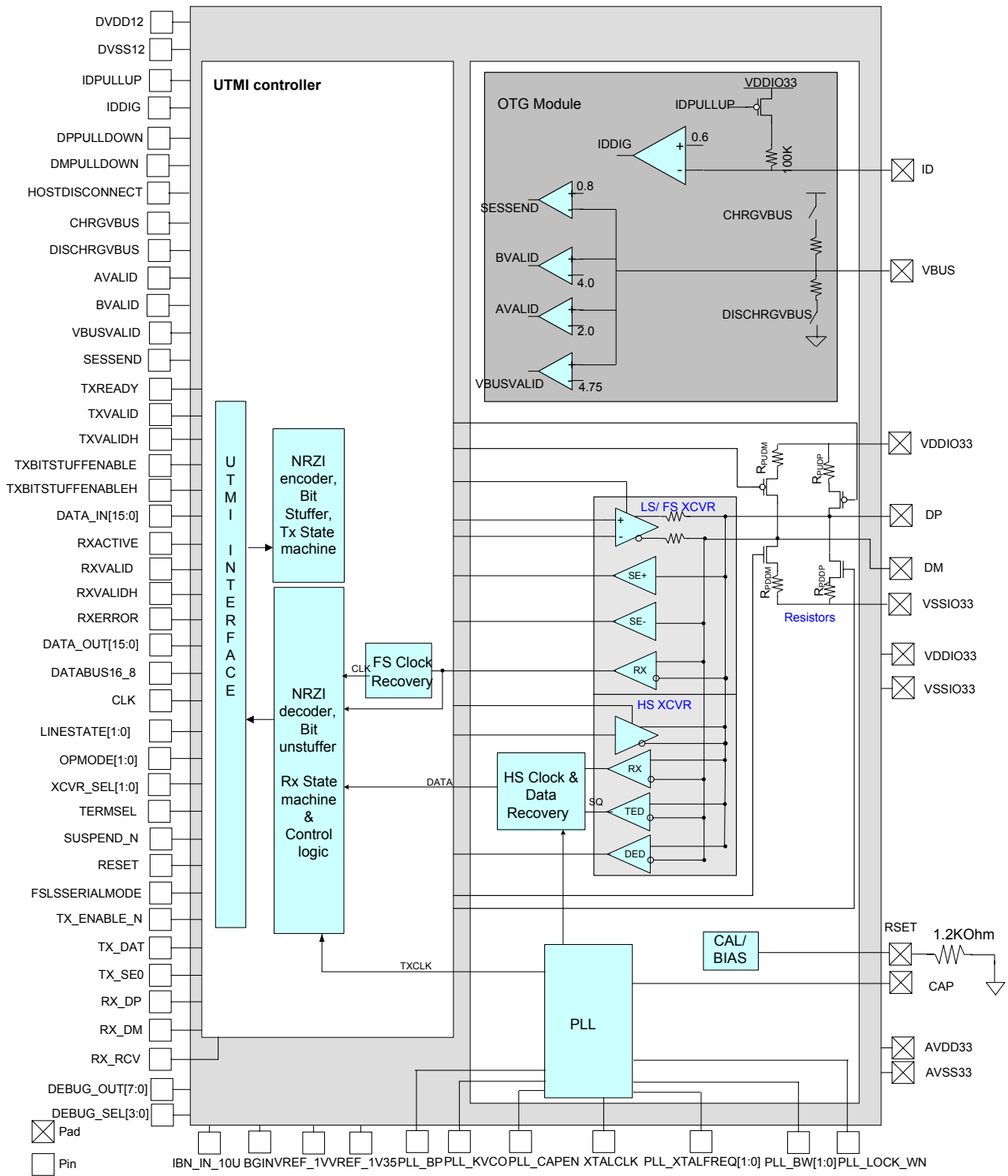


Figure 1. QCUSB1-09T Block Diagram

QCUSB1-09T

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Table 1. Operating Conditions

Parameter	Min	Typ	Max	Units
Analog power supply range (AVDD33)	2.97	3.3	3.63	V
Digital power supply range (VDDIO33)	2.97	3.3	3.63	V
Digital power supply range (DVDD12) ⁽¹⁾	0.90	1.0	1.1	V
Digital power supply range (DVDD12) ⁽²⁾	1.08	1.2	1.26	V
Band Gap Reference input (BGIN)	1.16	1.18	1.2	V
Input Reference Voltage (VREF_1V)	0.95	1	1.05	V
Input Reference Voltage (VREF_1V35)	1.3	1.35	1.4	V
Input Bias Current (IBN_IN_10U)	7	10	13	uA
XTALCLK Input Frequency	10	-	30	MHz
XTALCLK Input Jitter (Peak to Peak)	-	-	20	ps
Operating Junction Temperature	-40	25	125	°C
Storage Temperature	-65	25	150	°C

- (1) DVDD12 supply voltage for TSMC 90 G process
(2) DVDD12 supply voltage for TSMC 90 GOD process

Table 2. Electrical Characteristics

Parameter	Min	Typ	Max	Units
Total Power (Full speed Transmit), FS transmitting at 12Mb/s; 50pF load on DP and DM	29	32	33	mW
Total Power (Full speed Receive), FS receiving at 12Mb/s	8.0	8.5	10.5	mW
Total Power (Full speed Loop back), FS loop back at 12Mb/s; 50pF load on DP and DM	37	41	44	mW
Total Power (High speed Transmit), HS transmitting at 480Mb/s load	62	73	77	mW
Total Power (High speed Receive), HS receiving at 480Mb/s	8	10	13	mW
Total Power (High speed Loop back), HS transmitting into a 450ohm load	70	83	90	mW
Operating Supply Current (Suspend mode), 1.5K Ohm pull-up and 15K Ohm pull-down resistors on pin DP disconnected	-	-	50	uA
Operating Supply Current (Suspend mode), 1.5K Ohm pull-up and 15K Ohm pull-down resistors on pin DP connected	-	-	2.5	mA
Tx power supply current (I _{VDDIO33}), Full speed operation (12 Mb/s)	-	22	40	mA
Tx power supply current (I _{DVDD12}), Full speed operation (12 Mb/s)	-	0.2	0.5	mA
VDDIO33 power down current (I _{VDDIO33PD}), Full speed operation	-	1	-	uA
DVDD12 power down current (I _{DVDD12PD}), Full speed operation	-	1	-	uA
Hi-Z State Data Line Leakage (I _{LO}), Full speed operation (12 Mb/s)	-10	-	+10	uA
OFF-State Leakage Current (I _{LZ})	-	-	1	uA
Low-level input voltage, V _{IL}	-	-	0.20* DVDD12	V
High-level input voltage, V _{IH}	0.80* DVDD12	-	-	V
ESD Tolerance, Human Body Model ⁽¹⁾	2	-	-	KV
Latch-up Tolerance ⁽²⁾	150	-	-	mA
Input pin capacitance (Digital Inputs)	-	0.1	-	pF
Low speed/ Full Speed Receiver				
Receiver Low-level Input Voltage (V _{IL})			0.8	V
Receiver High-level Input Voltage (V _{IH})	2.0			V
Receiver High-level (Floating) Voltage (V _{IHZ})	2.7		3.6	V

QCUSB1-09T

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Parameter	Min	Typ	Max	Units
Receiver Differential Input Sensitivity (V_{DIFS})	0.2			V
Receiver Differential Input Common Mode Range (V_{CMFS})	0.8		2.5	V
Single-Ended Receiver Hysteresis Voltage (V_{HYSSE})	0.4		0.7	V
Low speed/ Full Speed Transmitter				
Transmitter Low-Level Voltage (V_{FSOL})	0.0		0.3	V
Transmitter High-Level Voltage (V_{FSOH})	2.8		3.6	V
Transmitter Single-Ended 1 (V_{OSE1})	0.8			V
Transmitter Signal Crossover Voltage (V_{CRS})	1.3		2.0	V
High Speed Receiver				
High-Speed Squelch detection threshold (Differential), Squelch detected, High Speed operation (480 Mb/s) V_{HSSQ}	-	-	100	mV
High-Speed Squelch detection threshold (Differential), No Squelch detected, High Speed operation (480 Mb/s) V_{HSSQ}	150	-	-	mV
V_{HSDI} high-speed differential input sensitivity $ VI(DP)-V(DM) $, High speed operation (480 Mb/s)	300	-	-	mV
V_{HSCM} high-speed data signaling common mode voltage range, High speed operation (480 Mb/s)	-50	200	500	mV
High Speed Transmitter				
Transmitter Low-Level Voltage (V_{HSOL})	-10		10	mV
Transmitter High-Level Voltage (V_{HSOH})	360		440	mV
High-Speed Idle Level (V_{HSOI})	-10		10	mV
Chirp-J Output voltage level (Differential) (V_{CHIRPJ})	700		1100	mV
Chirp-K Output voltage level (Differential) (V_{CHIRPK})	-900		-500	mV
Terminations				
FS Output Driver impedance for High-Speed PHY $Z_{HSDRV}^{(3)}$	40.5	45	49.5	Ω
Bus Pull-up resistor (R_{PU}), Bus IDLE	0.9	1.24	1.575	K Ω
Bus Pull-up resistor (R_{PU}), Device Receiving	1.425	2.26	3.090	K Ω
Bus Pull-down resistor (Z_{PD})	14.25	15	15.75	K Ω
Termination Voltage for upstream facing port pull-up (R_{PU})	3.0	3.3	3.6	V
Termination Voltage in High-Speed	-10		+10	mV
OTG Module Specifications				
A-Device Output VBUS voltage ($V_{A_VBUS_OUT}$)	4.4	-	5.25	V
A-Device Output VBUS current ($I_{A_VBUS_OUT}$)	8	-	-	mA
A-Device VBUS rise time ($T_{A_VBUS_OUT}$)	-	-	100	ms
A-Device Leakage Voltage ($V_{A_VBUS_LKG}$)	-	-	0.2	V
B-Device (SRP Capable) to OTG Device output voltage ($V_{B_OTG_OUT}$)	2.1	-	5.25	V
B-Device (SRP Capable) to Host output voltage ($V_{B_HST_OUT}$)	-	-	2.0	V
B-Device (SRP Capable) induced transient ($V_{B_DELTA_PK}$)	-	-	400	mV
VBUS Valid (V_{VBUS_VLD})	4.4	-	4.75	V
A-Device Session Valid ($V_{A_SESS_VLD}$)	0.8	-	2.0	V
B-Device Session Valid ($V_{B_SESS_VLD}$)	0.8	-	4.0	V
Session End Threshold (V_{SESS_END})	0.2	-	0.8	V
ID Pull-Up resistance ($IDPULLUP_N==0$) $R_{IDPULLUP}$	80	100	120	K Ω
ID Pull-Up resistance ($IDPULLUP_N==1$) $R_{IDPULLUP}$	1	-	-	M Ω
VBUS Pull-Up resistance R_{VBUS_PUP}	281	340	-	Ω
VBUS Pull-Down resistance R_{VBUS_PDN}	656	850	-	Ω

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- (1) Per MIL-STD-883C Method 3015.7
- (2) Per JEDEC JC-40.2
- (3) Includes internal matching resistors on both pins DP and DM. This tolerance range complies to Hi-Speed USB.

Table 3. Dynamic Characteristics (Timing Data)

Parameter	Symbol	Min	Typ	Max	Units
Low Speed Driver					
Rise Transition time	T_{LSR}	75	-	300	ns
Fall Transition time	T_{LSF}	75	-	300	ns
Rise and Fall time Matching	T_{LSRFM}	80	-	125	%
Full Speed Driver					
Rise Transition time	T_{FSR}	4	-	20	ns
Fall Transition time	T_{FSF}	4	-	20	ns
Rise and Fall time Matching	T_{FSRFM}	90	-	111.1	%
High Speed Driver					
Rise Transition time	T_{HSR}	500	-		ps
Fall Transition time	T_{HSF}	500	-		ps
Rise and Fall time Matching	T_{HSRFM}	90	-	111.1	%
Driver waveform Requirements (Eye pattern of Template 1 in USB2.0 specification)	-	See USB2.0 spec	-	-	
High Speed Receiver					
Receiver Waveform Requirements (Eye pattern of Template 4 in USB2.0 specification)	-	See USB2.0 spec	-	-	
Data Source Jitter and Receiver Jitter Tolerance (Eye pattern of Template 4 in USB2.0 specification)	-	See USB2.0 spec	-	-	
UTMI Interface timings					
Output Valid time on all Synchronous signals clocked with CLK	T_{VAL}	-	-	3	ns
Input Setup time for all Synchronous signals clocked with CLK	T_{SU}	-	-	2.5	ns
Input Hold time for all Synchronous signals clocked with CLK	T_{HLD}	-	-	2.5	ns