

# QCSSTL2CI3-13T



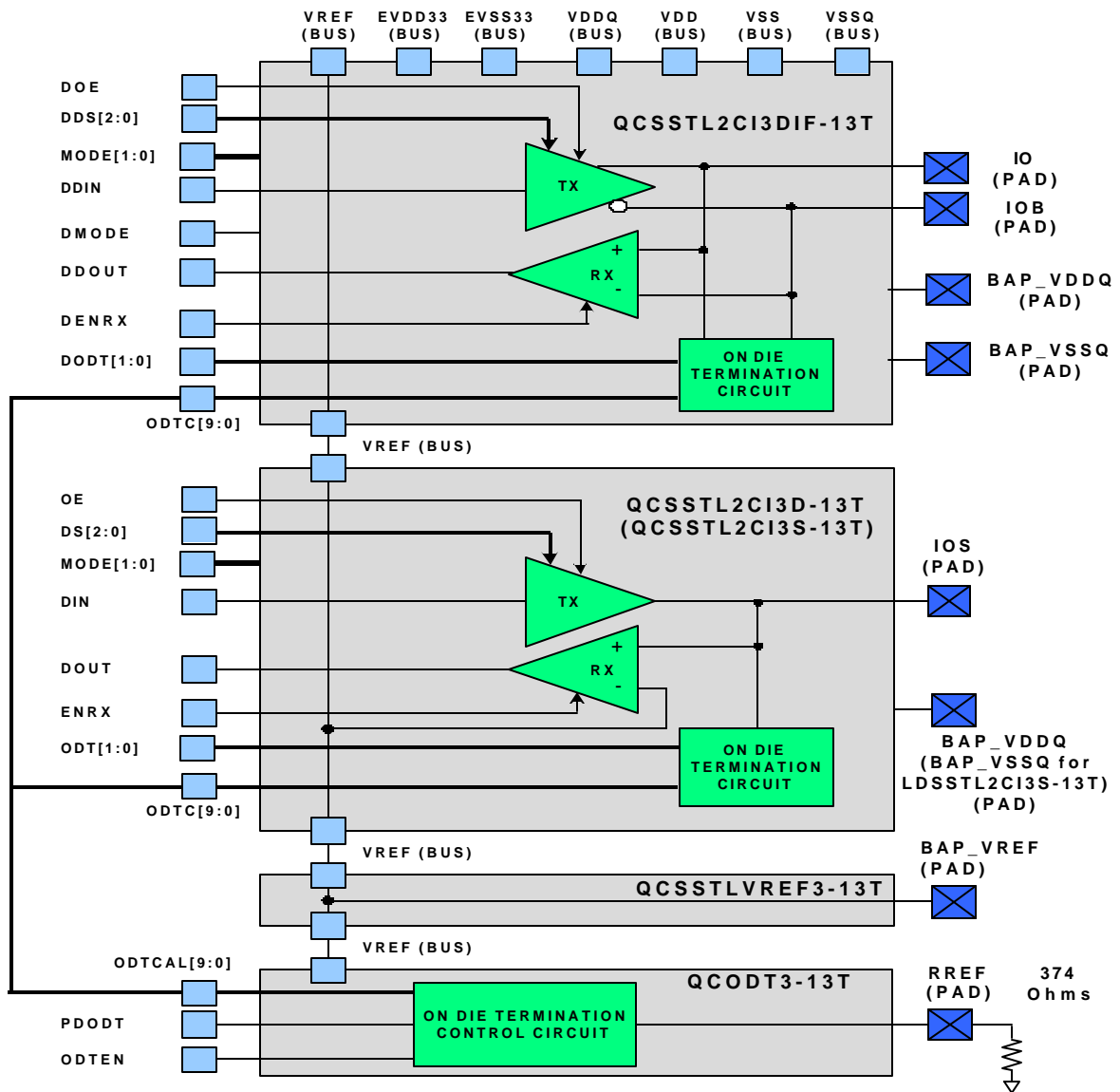
*Stub Series Terminated Logic (SSTL) 2.5V/1.8V Class  
I Transceiver, using 1.0V/3.3V FSG process*

## General Description

The QCSSTL2CI3-13T is a non-inverting SSTL 2 Class I 2.5v/1.8v Transceiver I/O that is compatible with JEDEC standards JESD8-9A and JESD8-15. Five separate cells make up the SSTL package, which includes the differential SSTL IO (QCSSTL2CI3DIF-13T), the single ended SSTL with VDDQ port (QCSSTL2CI3D-13T), the single ended SSTL with VSSQ port (QCSSTL2CI3S-13T), the VREF I/O (QCSSTLVREF3-13T) and the ODT Calibration I/O (QCODT3-13T).

## Features

- Cell uses 1P8M (M8 is thick)
- Designed for a 0.13 um, 1P8M 1.0V/3.3V FSG CMOS logic process
- Differential SSTL I/O Size – 140 um x 300 um
- Single Ended SSTL I/O Sizes - 70 um x 300 um
- VREF I/O size – 35 um x 300 um
- OTD Calibration I/O size – 105 um x 300 um
- 500 MHz operation into 5 pF load
- Programmable output drive strengths and ODT
- Supports SSTL2 Class I, SSTL18, GDDR-II



**Figure 1. QCSSTL2CI3-13T Block Diagram**