

QCSSTL183-065U



*Stub Series Terminated Logic (SSTL) for 1.8v and 2.5v Class I/
Class II Transceiver using 1.2v/2.5v, Logic Mixed Mode Low
Leakage process*

General Description

The QCSSTL183-065U is a SSTL 18 and SSTL 2 Class I/Class II non-inverting SSTL Transceiver I/O compatible with JEDEC standard JESD8-9B and JESD8-15A. Fourteen separate cells make up the SSTL package, which includes the differential SSTL I/O (QCSSTL183DIF-065U), the single ended SSTL port (QCSSTL183SE-065U), the VREF I/O (QCSSTLVREF183-065U) and the ODT Calibration I/O (QCODT183-065U). The remaining cells include the power/ground I/O's, a pad ring bus interface cell, filler cells and a corner cell.

Features

- Designed for a 0.065 μ m, 1P10M, Logic Mixed Mode, Low Leakage 1.2V/2.5V process
- Cell uses 1P6M
- Differential SSTL I/O Size – 70 μ m X 360 μ m
- Single Ended SSTL I/O Sizes - 35 μ m X 360 μ m
- ODT Calibration I/O size – 105 μ m X 360 μ m
- 533 MHz operation, in SSTL 18 mode(Mode1) and supports DDR2
- 266MHz operation in SSTL 2 mode(Mode2) supports DDR
- Programmable output drive strengths and ODT
- Antenna diodes for all digital inputs
- Pads incorporate ESD structures
- IO uses Rvt and Hvt MOS devices
- IO uses Bonded Over Active Circuit (BOAC) pad

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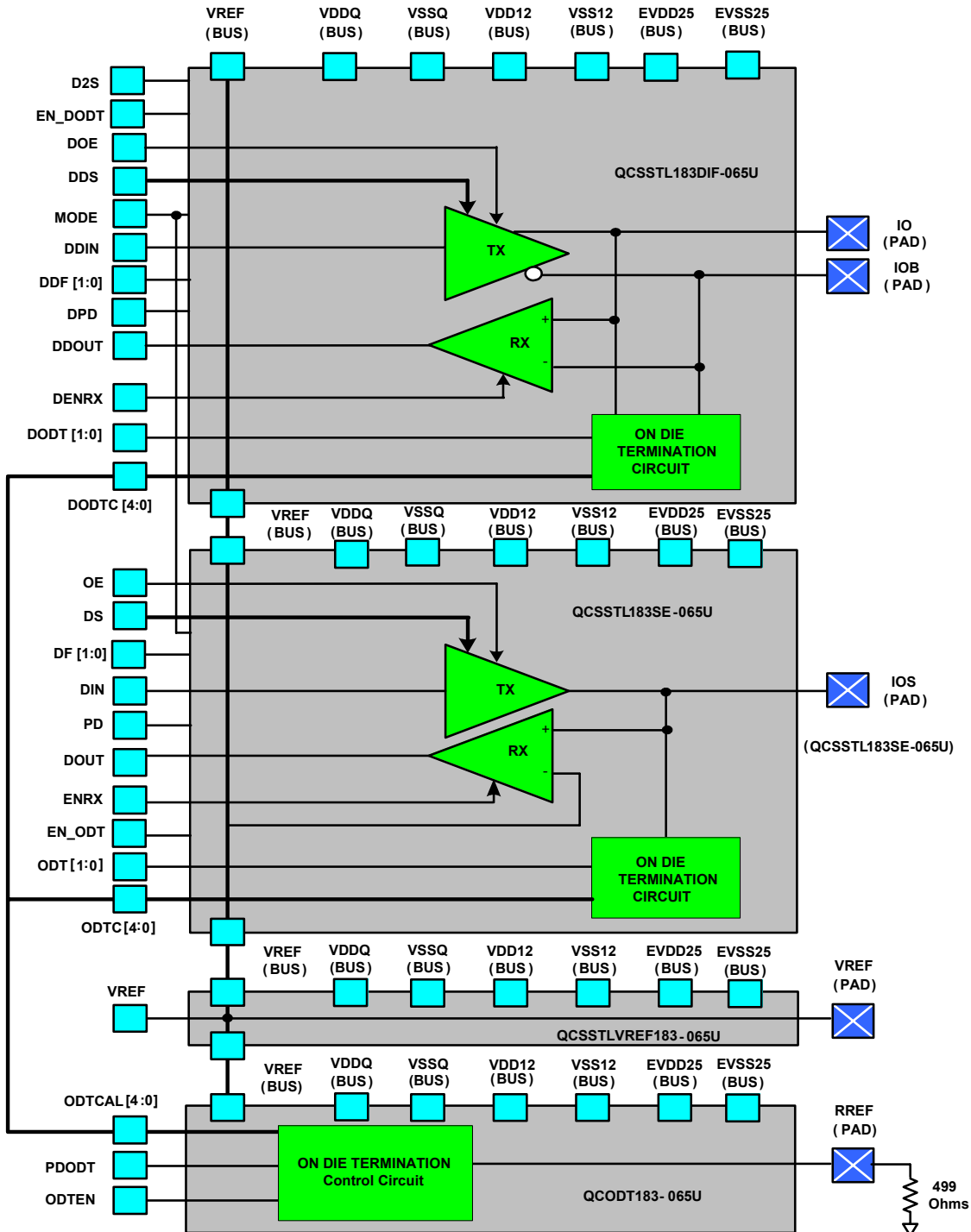


Figure 1. QCSSTL183-065U Block Diagram