

# QCPLL28-09T

50 to 150 MHz Spread Spectrum Phase-Locked Loop for digital clock synthesis using 1.0V/3.3V process



## General Description

The QCPLL28-09T cell is a phase-locked loop clock multiplier circuit that can generate a stable, high-speed Spread Spectrum clock from a slower clock signal. The cell integrates a voltage-controlled oscillator (VCO), a phase-frequency detector, a low pass filter and all associated support circuitry. The phase-locked loop cell operates when the powerdown signal (PD) is a logic level 0, and goes into a powerdown state when the powerdown signal is a logic level 1. A lock signal (LOCK) is provided which gives an indication of when the PLL is locked. The QCPLL28-09T cell is useful for clock multiplication of stable crystal oscillator sources.

## Features

- Designed for 1P8M, 90 nm 1.0V/3.3V CMOS generic logic process
- Cell uses 1P8M (M7 and M8 are thick)
- Small size – 550 um x 750 um
- 50 to 150 MHz operation
- Normal and Spread Spectrum modes
- Low power supply current
- Pin provided for powerdown mode
- Bypass mode built into PLL
- Ports on M3-M4
- Antenna diodes on all digital inputs
- Triangle down spread spectrum profile

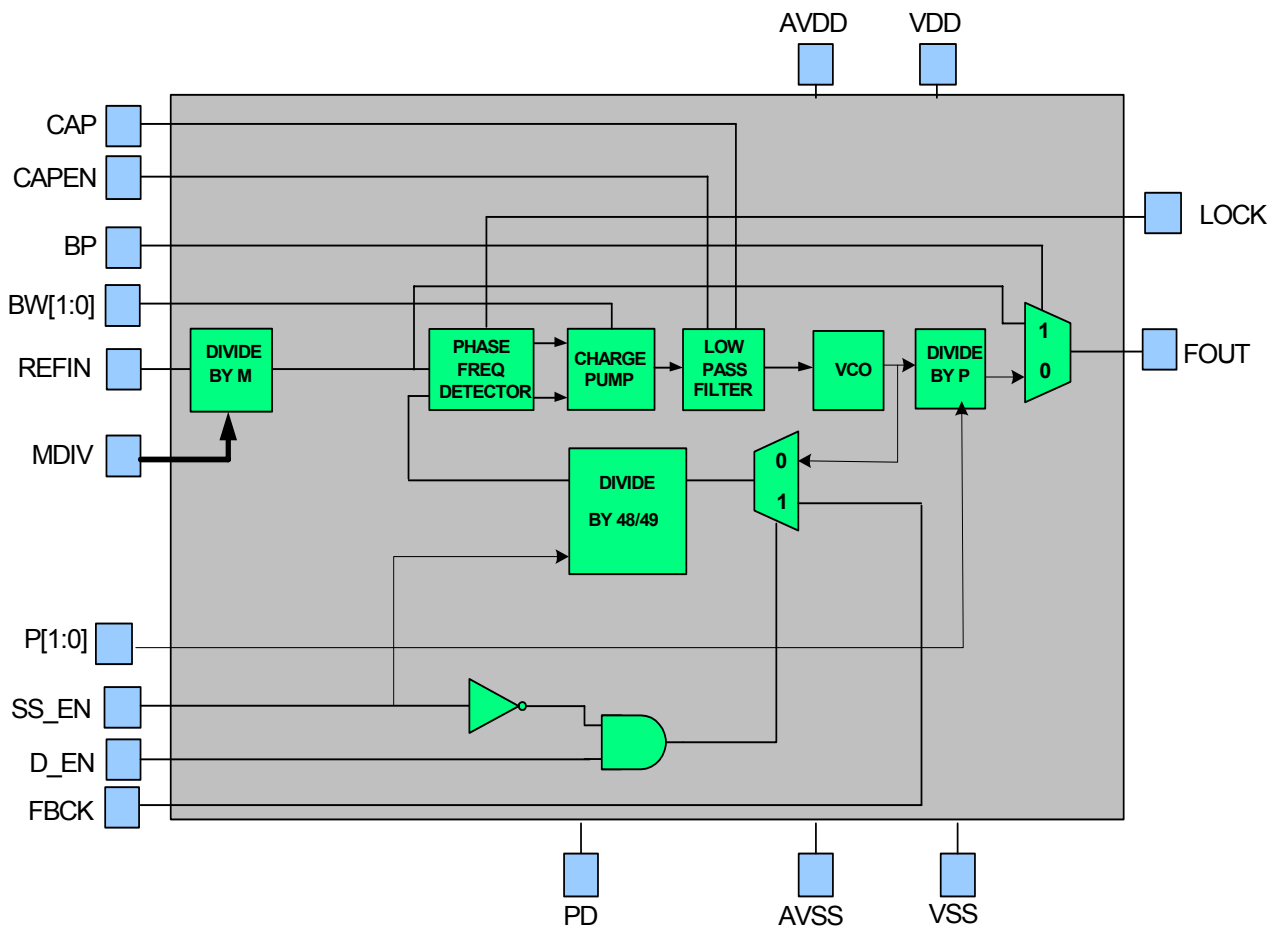


Figure 1. QCPLL28-09T Block Diagram