

QCLVDS11-18T

CMOS LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) TRANSCEIVER, 800 MHz, 1.8V PAD



General Description

The QCLVDS11-18T is a Transceiver that provides CMOS to LVDS then back to CMOS signal level translation. It provides a high-speed (800 MHz) data rate interface between devices operating at CMOS logic levels but communicating between each other at LVDS logic levels, thus assuring a high rate of data transfer. LVDS is a low swing, differential signaling technology. The low swing and current mode driver outputs create low noise and provide with very low power consumption across different frequencies. The QCLVDS11-18T Transceiver I/O is implemented in a 1P6M 0.18um CMOS Logic process, and consists of two separate IO's: Transmitter (QCLVDS11_18T_TX) and Receiver (QCLVDS11_18T_RX).

Features

- 0.18 um 1P6M Salicide 1.8V technology
- Cell uses 1P5M (M6 is thick but not used)
- Size: 200.0um x 313.0um (not including pad)
- Operates at speeds up to 800 MHz
- Integrated 100 Ohm resistor in receiver
- Utilizes standard CMOS process
- Powerdown mode for both IO's
- Output swing control (250-400mV or 100-300mV)
- Pads incorporate ESD structures
- Does not require ESD layer

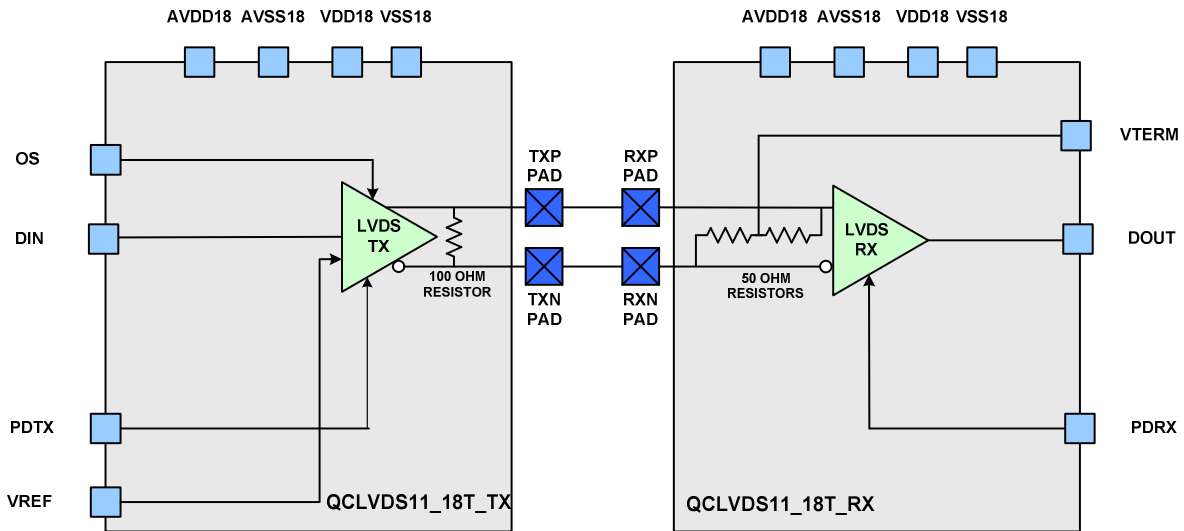


Figure 1. QCLVDS11-18T Block Diagram