

QCDLL5-13T



250 MHz to 500 MHz Delay-Locked Loop using
1.0V/3.3V FSG process

General Description

The QCDLL5-13T cell is a delay-locked loop circuit that can generate four stable, high-speed clock signals that are 90 degrees apart. The delay-locked loop cell operates when the powerdown signal (PD) is a logic level 0, and goes into a powerdown state when the powerdown signal is a logic level 1. A lock signal (LOCK) is provided which gives an indication of when the DLL is locked. Two separate cells make up the DLL package, which include a master DLL cell (QCDLL5-13T-M) and a single channel slave DLL cell (QCDLL5-13T-S or QCDLL5-13T-SR).

Features

- Designed for a 0.13 um, 1P8M, 1.0V/3.3V FSG CMOS process
- Cell uses 1P6M (M8 is thick, but not used)
- Master cell size – 300 um x 260 um
- QCDLL5-13T-S: Slave cell size – 35 um x 300 um
- QCDLL5-13T-SR: Slave cell size – 100um x 100um
- 250 MHz to 500 MHz operation
- 90 degree outputs
- External resistor (BGRSET) required
- DLL covered with shield on metal 6
- Single channel slave delay line

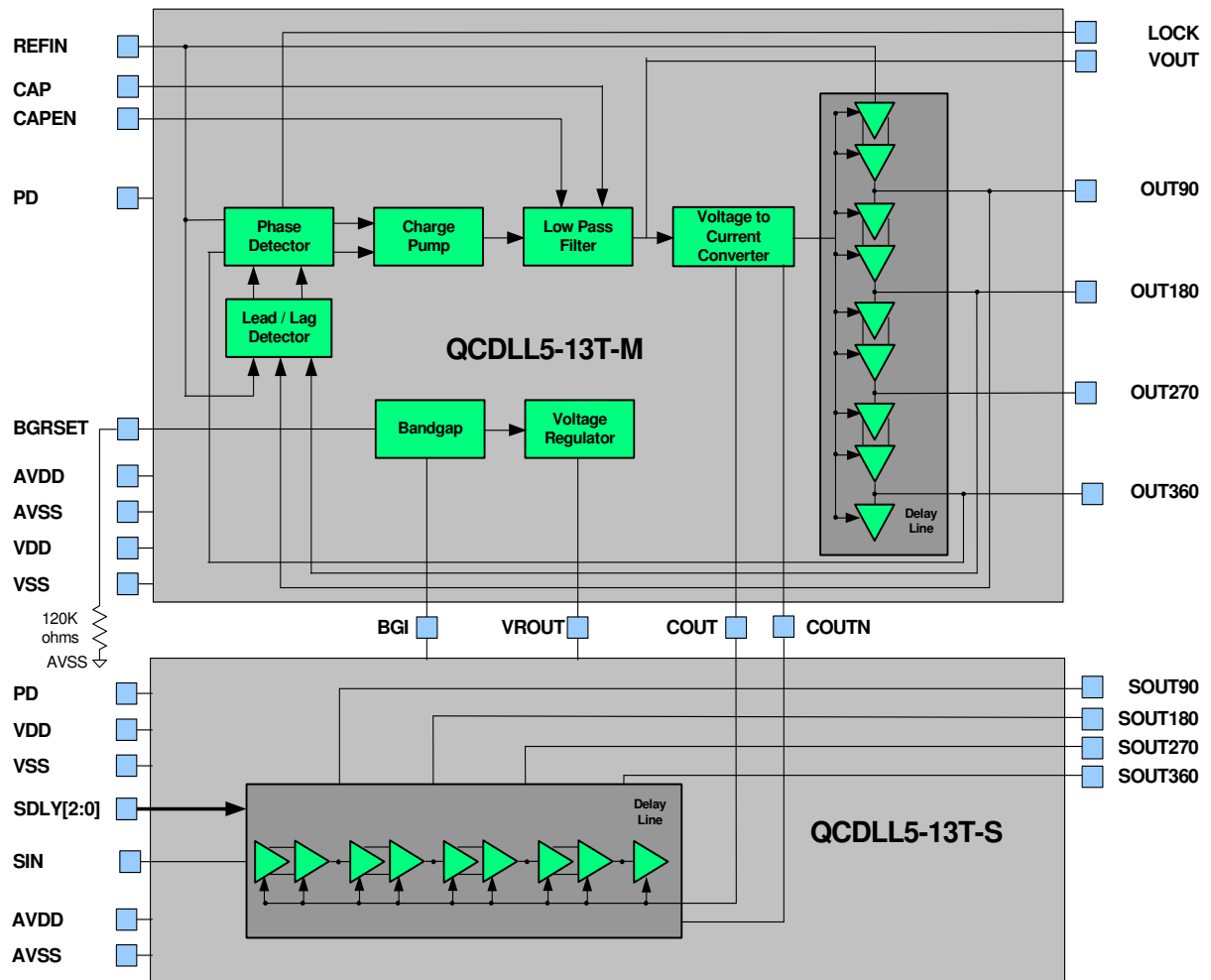


Figure 1. QCDLL5-13T Block Diagram