

QCDLL4-065U

200 MHz to 800 MHz Delay-Locked Loop



General Description

The QCDLL4-065U cell is a delay-locked loop circuit that can provide a 90 degree phase shift of data strobe from the reference clock. The delay-locked loop cell operates when the powerdown signal (PD12) is a logic level 0, and goes into a powerdown state when the powerdown signal is a logic level 1. A lock signal (LOCK) is provided which gives an indication of when the DLL is locked.

Features

- Designed for UMC 65nm Logic Mixed Mode, Low Leakage 1.0V/2.5V CMOS Process.
- Cell uses 1P6M
- Cell uses Deep N-well
- Master cell size – 400 um x 400 um
- Each Slave cell size – 200 um x 200 um
- Delay compensation cell size -
- 200 MHz to 800 MHz operation
- 90 degree output with 64 steps phase select at Slave
- Ports on M3-M6
- Antenna diodes on all digital inputs

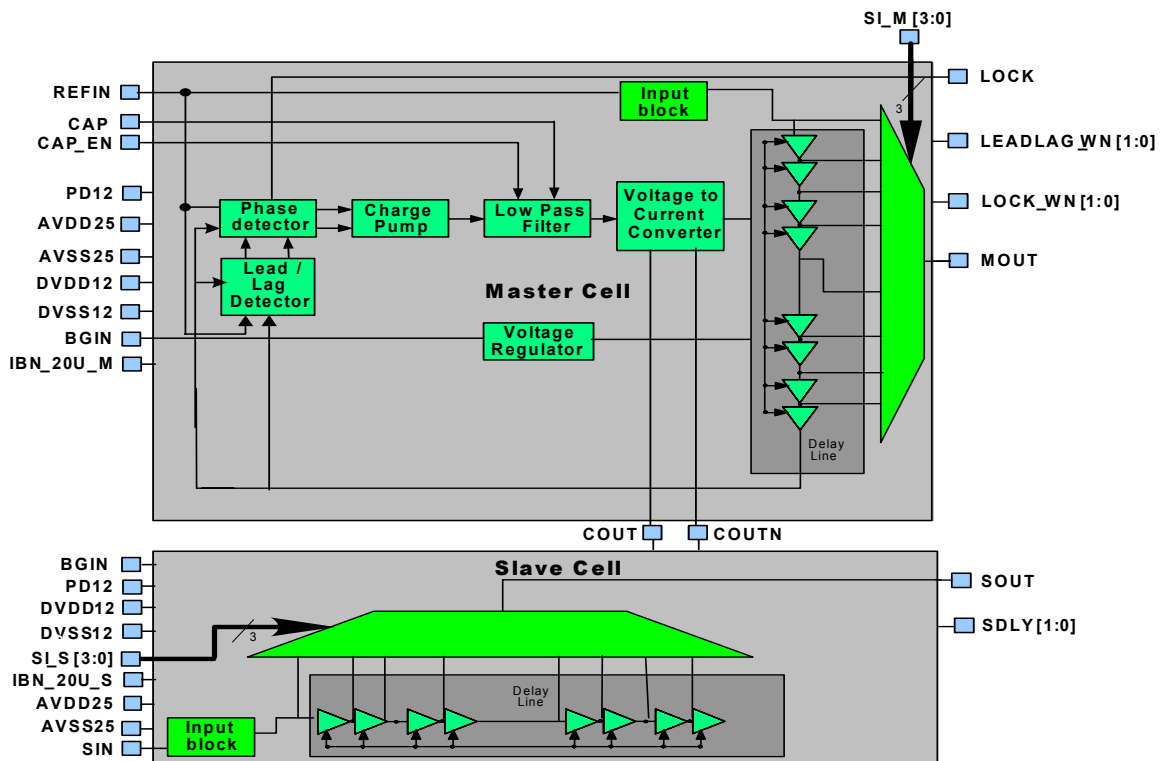


Figure 1. QCDLL4-065U Block Diagram