

QCDDR12-065U



**200 MHz (400 Mbps/pin) DDR SDRAM / 533MHz
(1066Mbps/pin) DDR-II SDRAM Interface for
1.2V/2.5V Low Leakage process**

General Description

The QCDDR12-065U cell is a DDR/DDR2-SDRAM interface circuit which supports 16 bit wide DDR/DDR2 (8Mbit x 16 data bits x 4 banks). The QCDDR12-065U cell can operate either in DDR/ DDR2 Mode depending upon the external mode control pin.

In DDR Mode the interface utilizes a 2n pre-fetch architecture, which transfers two data words per clock cycle on both the sides of the interface, such that the clock rate on both sides of the interface is same.

In DDR2 mode the interface utilizes a 4n pre-fetch architecture, which transfers two data words per clock cycle, such that four data words are read from the memory device during a read cycle. In DDR2 Mode the core clock frequency is half of the frequency of the Memory interface.

The interface has a Master DLL and multiple slave DLL's to align the read strobes at the center of the valid read data window. The data and read data valid strobe are then transferred to the application core, all aligned to the rising edge of the application's (core) internal clock.

The write data is coming from the application in 32/64 bits widths, together with the mask and valid signals, all of which are aligned to the rising edge of the application's internal clock.

The QCDDR12-065U cell uses SSTL2 Class II I/O's for the memory interface signals in DDR Mode and SSTL18 I/O's for the memory interface signals in DDR-II mode.

Features

- Designed for a 65nm, 1P10M 1.2V/2.5V Logic Mixed mode Low Leakage (LL) Process
- Cell uses 1P6M
- DDR Slice 0 / DDR Slice1 size –0.7 sqmm.
- DDR Command and Address block size – 1.26sqmm.
- Timing and Synchronization block (Including PLL) size – 0.25sqmm.
- BGB And Bias Block Size – 0.042sqmm
- Compatible with DDR / DDR-II Memory interface
- Maximum 533 MHz operation in DDR-II mode/ 200MHz operation in DDR Mode
- Bi-directional strobe signals
- Core ports on M2 – M5
- Antenna diodes on all core digital inputs
- Embedded registers scan support
- Compliant with DDR SDRAM Jedec standard JESD79E
- Compliant with DDR-II SDRAM Jedec standard JESD79-2C
- Option for On Die Termination or Mother Board Termination
- DDR/DDR-II Macro uses Rvt and Hvt MOS devices
- DDR/DDR-II Macro uses Bonded Over Active Circuit pad type for all the SSTL I/Os on Memory side

QCDDRII2-065U



200 MHz (400 Mbps/pin) DDR SDRAM / 533MHz
 (1066Mbps/pin) DDR-II SDRAM Interface for
 1.2V/2.5V Low Leakage process

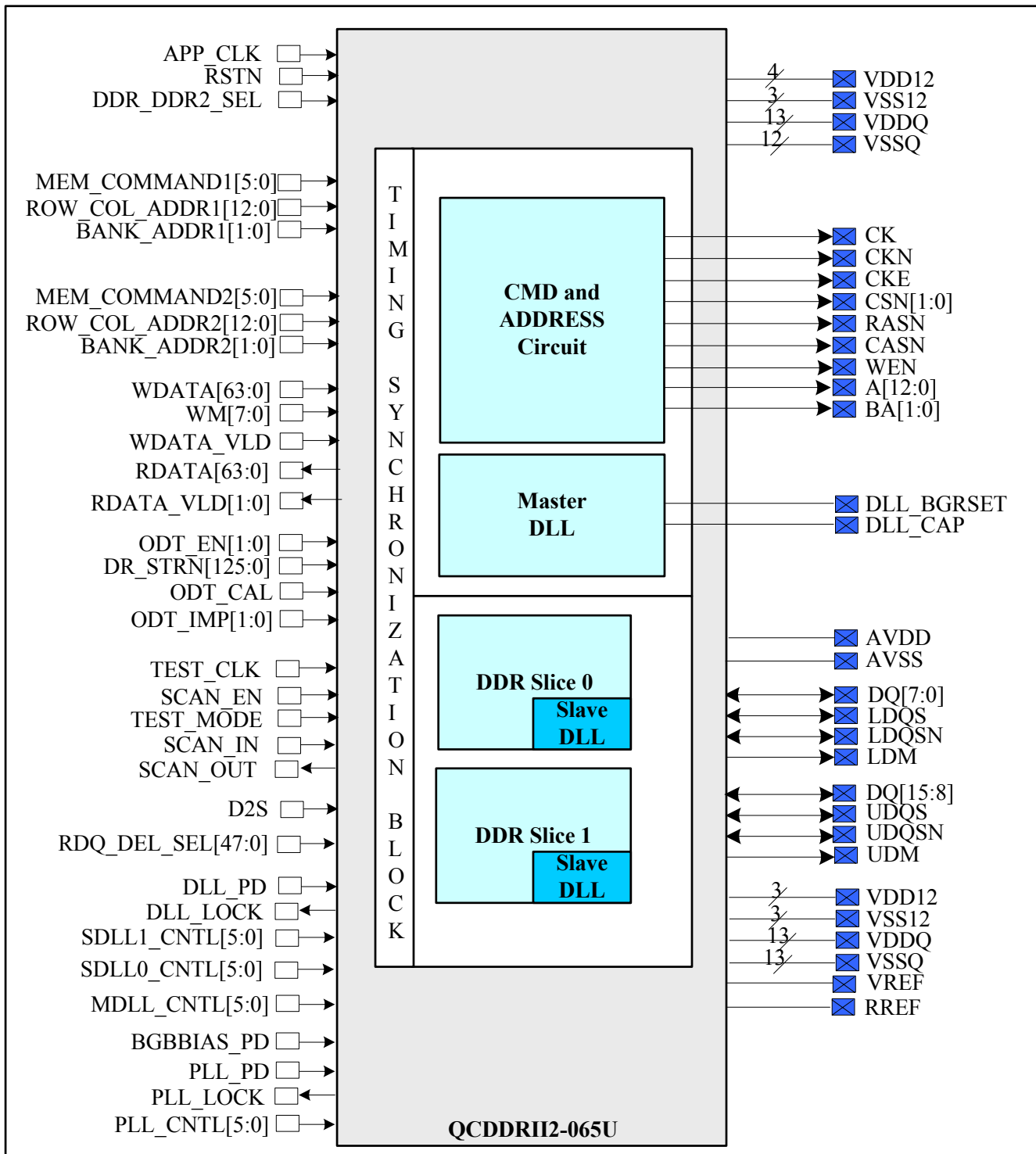


Figure1. QCDDRII2-065U Block Diagram