



M16550OCP UART Controller with OCP Interface

Features

- Programmable serial interface parameters including number of bits per character, even/odd/no parity, number of stop bits and baud rate.
- Sixteen-byte deep transmit and receive FIFOs.
- Programmable interrupt enabling for interrupts generated from transmitter/receiver/line status and modem status.
- Line break generation, detection and reporting.
- Internal diagnostic capabilities with loopback control, break, parity, overrun and framing error generation and detection.
- Prioritized interrupt control
- Modem handshake control and status reporting.
- Programmable Receive FIFO threshold to improve throughput.
- Synchronous CPU interface.
- Fully synchronous design making it DFT friendly
- The Megacell can be kept in test mode by asserting TST_MODE.

Functional Overview

M16550OCP performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART through OCP interface at any time during the functional operation. It provides modem handshake through input and output signals for easy interfacing with modems during communication. The design is fully synchronous making it DFT friendly and enables ease of integration in a SOC application.

Sixteen-byte deep transmit and receive FIFOs and programmable threshold on the receive FIFO allows the system designer to program the core for optimized throughput. Interrupt and error reporting capabilities add to ease of use.

Self-diagnostic capabilities like internal loopback and line error generation and detection facilitates location of faults and eases validation of the design. The 16-bit programmable baud rate generator permits the required baud rate to be generated from the system clock.

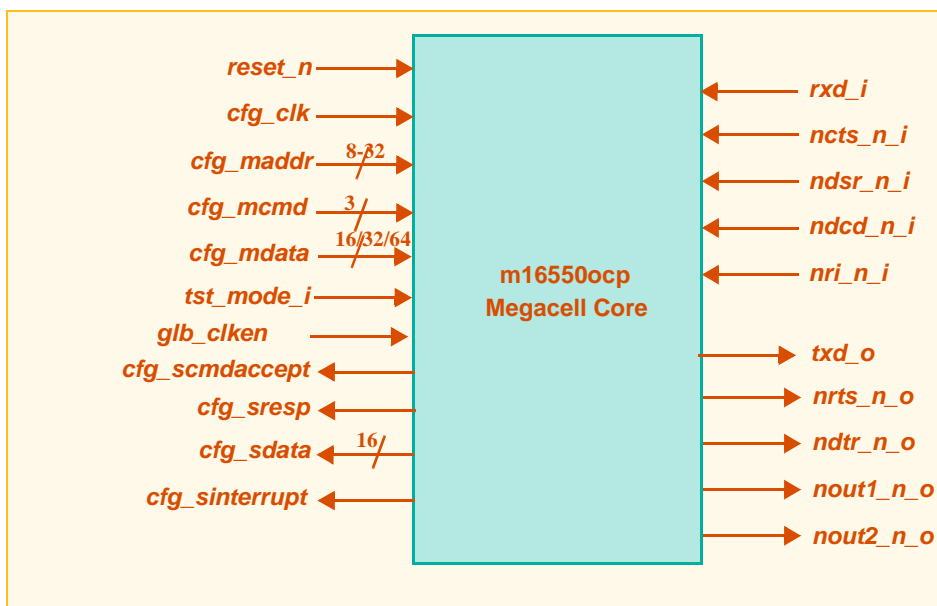


Fig 1: m16550ocp I/O Diagram

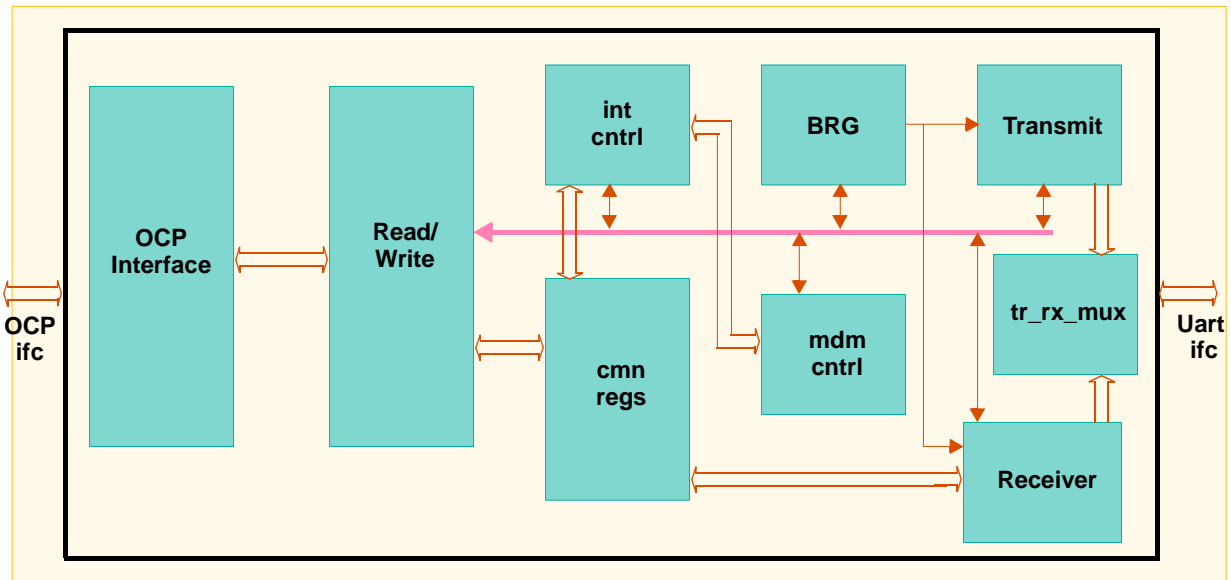


Fig 2: m16550ocp Block Level Diagram

Performance

| Parameter | Value | Remarks |
|----------------|--------|--|
| Gate Count | 5.5k | Approximate |
| Code Coverage | 100% | Block & Arc coverage, with Sure Cov tool. |
| OpenMORE Score | 96% | |
| Technology | 0.18u | TSMC Artisan |
| Frequency | 150MHz | Pre-route STA with Synopsys Design Compiler. |

Target Applications

- Typical SOC/embedded applications requiring an asynchronous serial communication controller.

Test Coverage

- 100% With Fastscan

Deliverables

- Fully synthesizable Verilog RTL.
- Documentation - Data Sheet, User Guide, Verification Description Document.
- Self checking Verification Suite.
- Synthesis and STA Script files.
- DFT Scripts.

Related Products

- M16550 - A standard part compatible design with Asynchronous CPU interface (National 16550)
- M16550S - A standard part compatible design with Synchronous CPU interface.
- M16450S - A standard part compatible design with Synchronous CPU Interface
- M16550APB - UART with APB interface

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