



V8051TCX

Configurable 8-bit Microcontroller

Features

- Instruction set fully compatible with Intel 8051
- Internal 256-Byte scratch pad RAM space and 128-Byte SFR address space
- Supports low power modes like Power down and Idle
- Supports On Circuit Emulation (ONCE)
- Timed access protection for certain SFR bits
- Supports standard mode features like
 - Serial Port
 - Three functionally different 16-bit timers
 - Two level interrupt structure with maximum six interrupt sources
- Supports turbo mode features like
 - Additional data pointer
 - Programmable length of MOVX memory access cycle to handle fast and slow memories/ peripherals
 - Power fail interrupt
 - Unused opcode A5 as DEC DPTR
 - Three level priority interrupt structure with maximum eight interrupt sources
 - Watch Dog Timer
- Configurability to select standard mode or turbo mode
- Configurable Extended Memory Mode to address up to 16MB of Program and Data Memory which supports
 - 16-bit Normal, 24-bit Paged and Contiguous addressing modes
 - Additional SFRs and Extended Data pointer for addressing Program memory and data memory upto 16MB each
 - Additional address lines on Port 4
- Configurability to have Internal Data memory of 4KB and Programmability to have extended stack of 1KB in internal data memory

Functional Overview

The V8051TCX is fully instruction set compatible to Intel 8051 and provides all the external interface signals that standard core provides. V8051TCX is configurable to add turbo and Extended Memory Mode features to standard 8051 core. A typical interface of the core with memories is shown in Fig 1: V8051TCX Interface with External Memories

The standard 8051 machine cycle is of 12 clock cycles and turbo version of 8051 takes 4 clock cycles per machine cycle. In turbo version, length of memory access due to MOVX instruction can be programmed between 2 to 9 machine cycles to work efficiently with both fast and slow memories/ peripherals.

In Extended Memory Mode, V8051TCX can be programmed to operate in normal (64KB) mode or extended mode (paged or contiguous addressing mode upto 16MB).

The core can be configured to integrate with internal RAM for Data memory up to 4KB. The core can be programmed to utilize lower 1KB of internal data memory for stack operations.

The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection. The megacell core provides three 16-bit timers that are functionally similar to the timers of the standard 805x series microcontrollers. Watchdog timer in turbo version can be used as a System Monitor or a very long time period timer. The turbo version of V8051TCX has a three level priority interrupt structure with maximum 8 interrupt sources and standard version has a two level interrupt

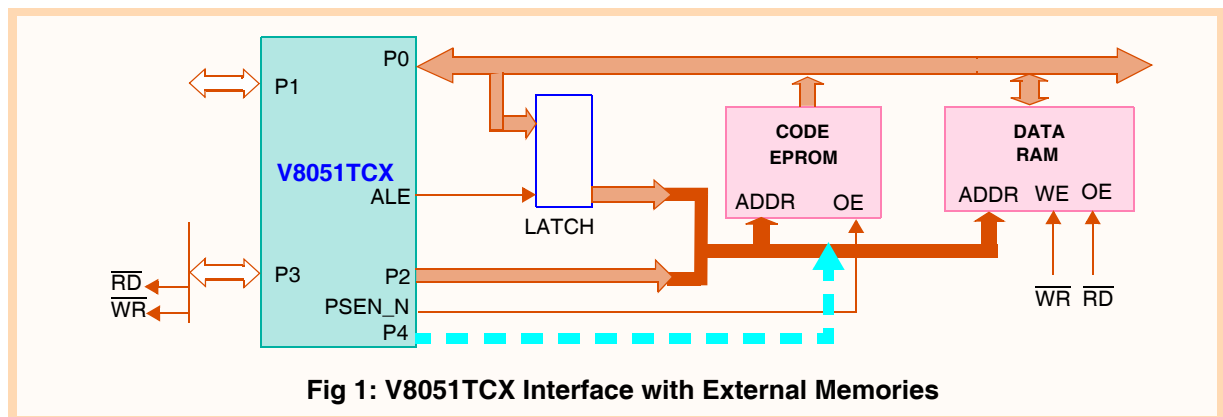


Fig 1: V8051TCX Interface with External Memories

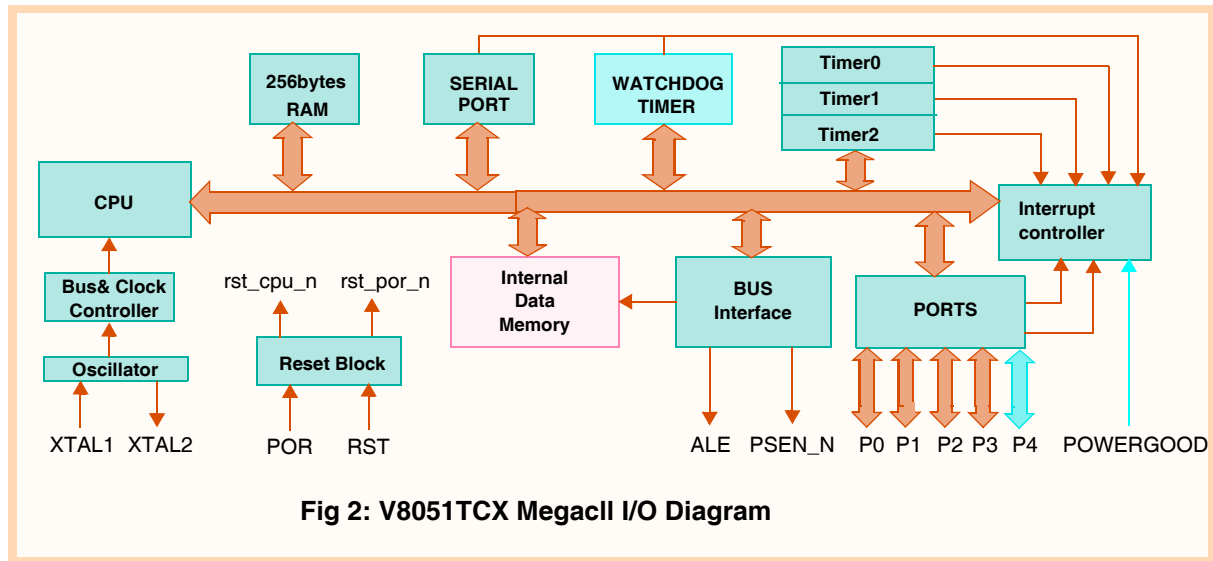


Fig 2: V8051TCX MegaCell I/O Diagram

priority structure with maximum of 6 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled. The I/O interface of the Core is shown in Fig 2: V8051TCX MegaCell I/O Diagram

V8051TCX has IDLE and POWERDOWN modes of operation. In the IDLE mode, the CPU's state machine is stopped while the timers, serial port and interrupt block continue to operate. In the POWERDOWN mode, clock to CPU as well as Peripheral blocks are stopped. This is the lowest power consumption state. The turbo version of the megacell provides a high priority non-maskable interrupt that can be connected to a Power-Fail circuit indicating an imminent power failure, so that user is given sufficient time to save critical data.

Performance Specifications

Parameter	Value	Remarks
Gate Count	~9K - 12K	standard mode Turbo mode with extended features
Code Coverage	100%	Block, Arc, State Transitions, Expressions, Events
OpenMORE Score	96%	
Technology	0.18μ	Artisan, TSMC
Frequency	97MHz	STA verified with pre-route, pre-scan netlist (internal timing performance with internal RAMs)

Target Applications

- All 8051 based general purpose applications
- In SoC designs with requirement for 8051 like controllers

Test Coverage

- Design is highly synchronous and scan friendly
- Fault coverage is 94% with ATPG vectors

Deliverables

- Fully synthesizable Verilog RTL source code
- Documentation - Data Sheet, User Guide, Verification Description Document
- Self checking Verification Suite
- Synthesis Scripts
- Scripts for STA & DFT (optional)

Additional Items

- Xilinx FPGA bitmap file for Virtex XCV1000E device for standard configuration

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