



V8102 - Xtensa to AHB wrapper interface (XWI)

Features

- Xtensa Read data bus configuration (32/64/128 bits)
- Xtensa Write data bus configuration (32/64/128 bits)
- AHB buswidth configuration (32/64/128 bits)
- Asymmetrical Xtensa Read/Write data bus widths
- Asymmetrical Xtensa and AHB bus widths
- Different Clock ratios (only Synchronous)
- Split/Retry transaction support on AHB bus
- Partial-word and Burst read support for Xtensa
- Partial-word write support for Xtensa
- Configurable Outstanding Write request buffering for Xtensa
- Read data buffering to support asymmetrical bus widths
- Configurable endianness support
- Early terminated transaction support
- Write transaction error indication support

Functional Overview

v802 is an Xtensa to AHB wrapper interface is interface between Xtensa processor and AHB devices. The megacell converts the request of Xtensa processor to AHB request, and acts as a master on AHB bus.

The core provides transactions read from, and write to different AHB slaves. The megacell is configurable for different configurations.

The megacell supports partial stream writes, partial reads and block read transactions. Megacell supports critical word first addressing in case of block reads. On AHB, depending on the scheme of arbitration Arbiter can remove grant at time. The core supports terminated transactions to take care above condition.

The megacell supports data packing, in case of asymmetrical BData/AHB bus widths.

The megacell's connection in a typical environment is shown in Fig. 1. The external interfaces to the megacell are indicated in Fig. 2.

The megacell is available as a fully synthesizable RTL design in Verilog and can be targeted to any vendor specific library.

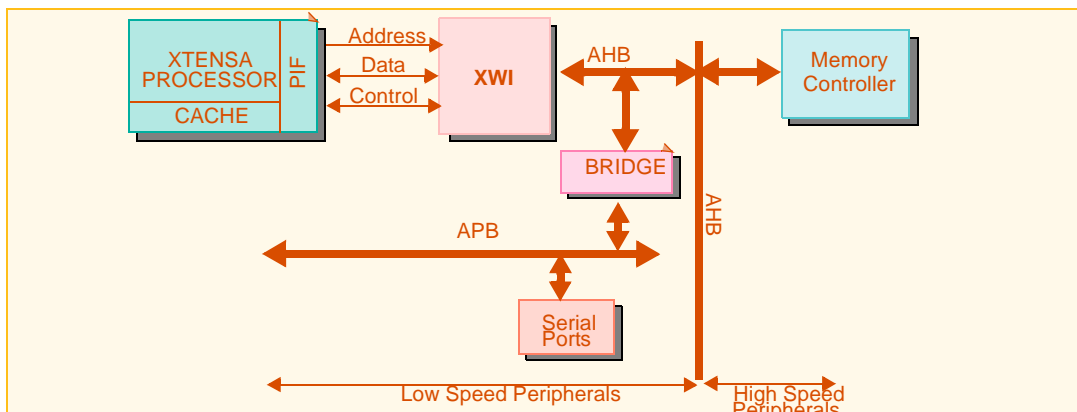


Fig 1: V8102 core in a typical system

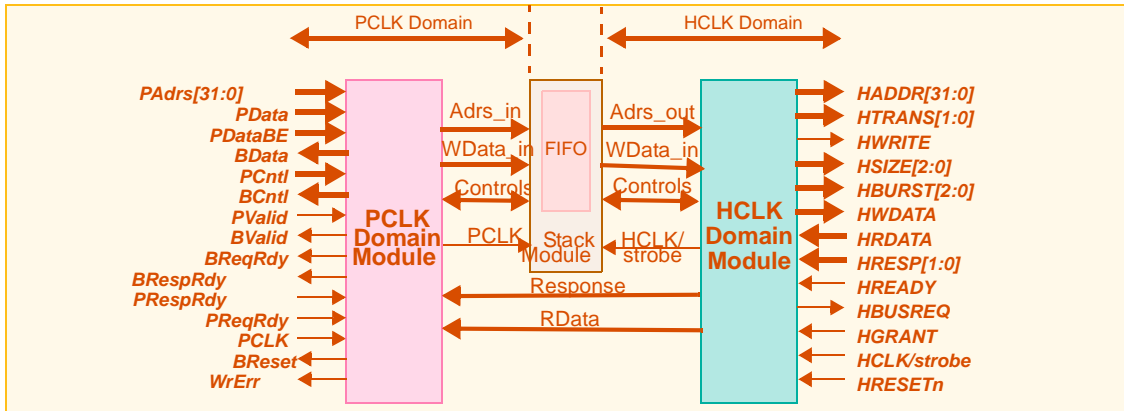


Fig 2: V8102 Megacell Core Block Diagram

Performance

Parameter	Value	Remarks
Gate Count	15 K	Including FIFOS, targeted to 0.18u technology with 32-32-32 bus configuration with fifo depth 16
Power Estimate		
Code Coverage	97.7%	
OpenMORE Score	91%	
IP Catalyst Rating	Gold	
Technology	0.18μ	Library :TSMC 0.18μ (slow.db)
Frequency	200:100 MHz	PCLK:HCLK (without scan)

Target Applications

- As a Bridge between Xtensa processor and AHB devices

Test Coverage

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List of Deliverables

- Synthesizable Verilog RTL source
- Synthesis scripts and timing constraints documents.
- Test bench and verification vectors.
- User guide

Related Products

- V8101 - AHB Based Memory controller
- V9301 - Enhanced Synchronous Serial Interface on APB (ESSI)
- V6001 - AHB to APB interface bridge
- M16550APB - UART with APB interface
- M146818APB - Real Time clock with APB interface
- V8001 - General Purpose Timer with APB interface
- V8002 - Watch Dog Timer with APB interface
- M8254APB - Programmable Interval Timer with APB interface

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