

## Features

- Supports eight memory devices of different types - SDRAM and CSI interfaces such as ROM, Flash and GPIO
- Addressing support upto 4GB memory
- AMBA-AHB, 32-bit compatible bus
- Support for AHB single beat, 4 beat and 8 beat wrapping bursts and Split transaction
- Read and Write data buffering
- APB Interface for configuration
- Upto 100MHZ SDRAM (32-bit) devices can be interfaced
- Supports byte and halfword writes to 32-bit SDRAM chips
- Transaction pipelining support with SDRAM
- Support for Auto-Refresh and Self-Refresh
- Paging Support for upto 4 open pages
- Parity generation and checking
- Support for interfacing with 8,16 and 32-bit CSI devices
- Burst read and write support for ROM and Flash interfaces
- Programmable read and write latency on a chip select basis
- Read Burst Acceleration for burst capable ROMs
- Write byte enables for writing lower width data into higher width GPIO devices
- Provides support for two types of modes with GPIO devices - Address strobe mode and Handshake mode

## Functional Overview

V8101 is an AHB based memory controller that can be interfaced with SDRAM, ROM, Flash and GPIO (General Purpose I/O) memory devices. The megacell acts as a slave on AHB bus.

The core provides all the functionality for read, write transactions from multiple masters to any interfaced memory device. The design makes the AHB, free from the read, write latencies of the memory devices by split transaction support and thus increases the bus utilization.

The megacell's operation can be controlled through programmable registers. The megacell provides APB interface to access these registers.

The megacell's connection in a typical AHB based environment is shown in Fig. 1. The external interfaces to the megacell are indicated in Fig. 2.

The megacell is available as a fully synthesizable RTL design in Verilog and can be targeted to any vendor specific library.

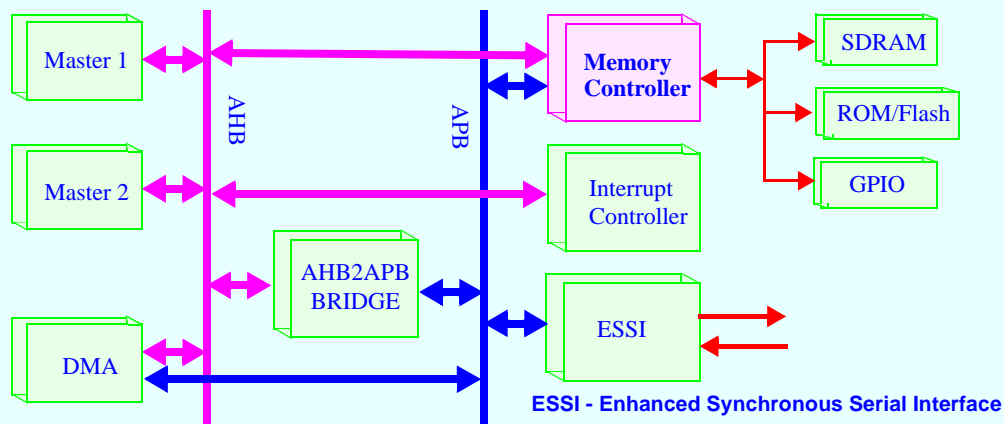


Fig.1 : V8101 in a typical environment

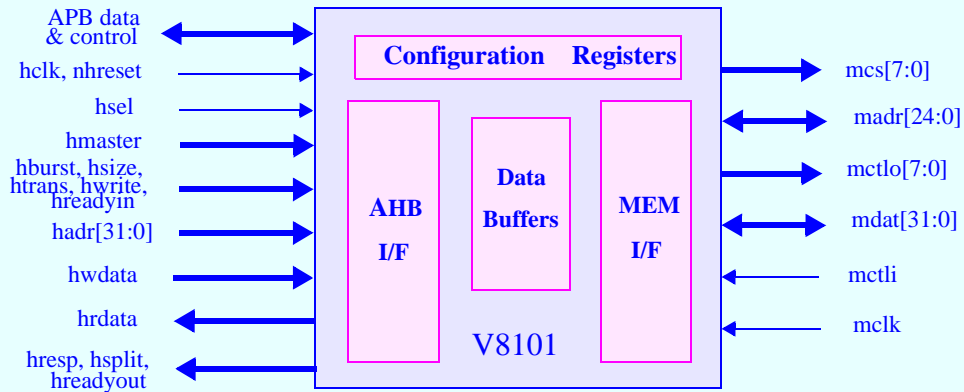


Fig. 2 : V8101 Megacell Core Block Diagram

## Performance

Parameter	Value	Remarks
Gate Count	42 K	Including FIFOS, targeted to 0.18u technology
Power Estimate	81mW	Targeted to 0.18u technology HCLK:MCLK=200MHz:100MHz
Code Coverage	78%	
OpenMORE Score	90%	
IP Catalyst Rating	TBD	
Technology	0.25 Micron	Library : PASSPORT 0.25u (cb25os163_generic_max.db)
Frequency	100 MHz	without scan

## Target Applications

- Memory controller in SOCs with AHB as internal bus

## Test Coverage

- 99% Fault coverage with APTG vectors on scan inserted netlist

## List of Deliverables

- Synthesizable Verilog RTL source
- Synthesis scripts and timing constraints documents.
- Script for scan insertion.
- Test bench and verification vectors.
- Bus monitors used in test bench.
- User guide
- Installation scripts

## Related Products

- V9301 - Enhanced Synchronous Serial Interface on APB (ESSI)
- V6001 - AHB to APB interface bridge
- M16550APB - UART with APB interface
- M146818APB - Real Time clock with APB interface
- V8001 - General Purpose Timer with APB interface
- V8002 - Watch Dog Timer with APB interface
- M8254APB - Programmable Interval Timer with APB interface
- V8102 - AHB Wrapper for Xtensa RISC CPU

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