



V1002X Xtensa CPU Interface Unit

Features

- Provides direct interface to Xtensa Processor Interface Bus, i.e., PIF.
- Provides interface to OCP Simple Extensions compliant System Bus.
- Provides interface to OCP Basic compliant Configuration Bus.
- Design can be created for Configuration and System Bus widths of 8/16/32/64 bits.
- Design can be created for PIF Bus width of 32/64 bits
- Provides appropriate synchronization between Xtensa CPU and System clock domains.
- Design can be created for connection to multiple peripherals upto a maximum of 16, on Configuration bus.
- Provides Configurable address map decoding for all IO peripherals to be integrated with Xtensa CPU in an SoC.

Functional Overview

The V1002X is designed to interface Xtensa Processor's PIF bus to OCP compliant bus. The core supports all possible transactions associated with movement of data between Xtensa CPU and the peripheral units used in an SoC. Fig 1: V1002X, XIU Core in a Typical SOC shows connection of V1002X in a typical SoC. The XIU handles the configuration space transactions between Xtensa CPU and IO peripherals and Memory data transfers between the Xtensa CPU and System Memory, based on the definition of System address map. XIU on one side interfaces to Xtensa PIF Bus and on the other side interfaces to OCP Basic compliant Configuration Bus and OCP Simple Extensions compliant System Bus. A suitable wrapper to OCP bus can be easily implemented to connect to any on-chip bus. XIU is the only master on the Configuration bus and is one of the masters on the System Bus.

The core implements major blocks like Clock synchroniser to provide synchronization between CPU clock and System clock domains, PBIU for handling PIF bus protocol, CBIU and SBIU blocks to communicate on Configuration and System Buses of SoC.

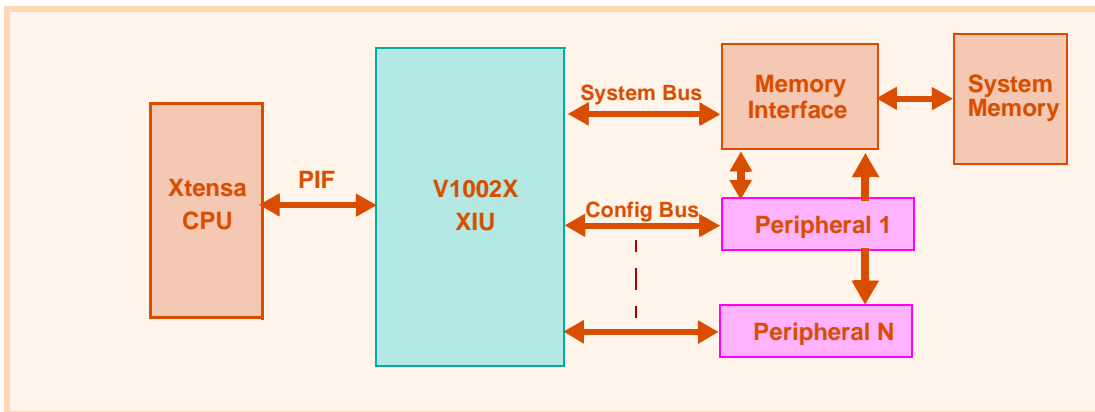


Fig 1: V1002X, XIU Core in a Typical SOC

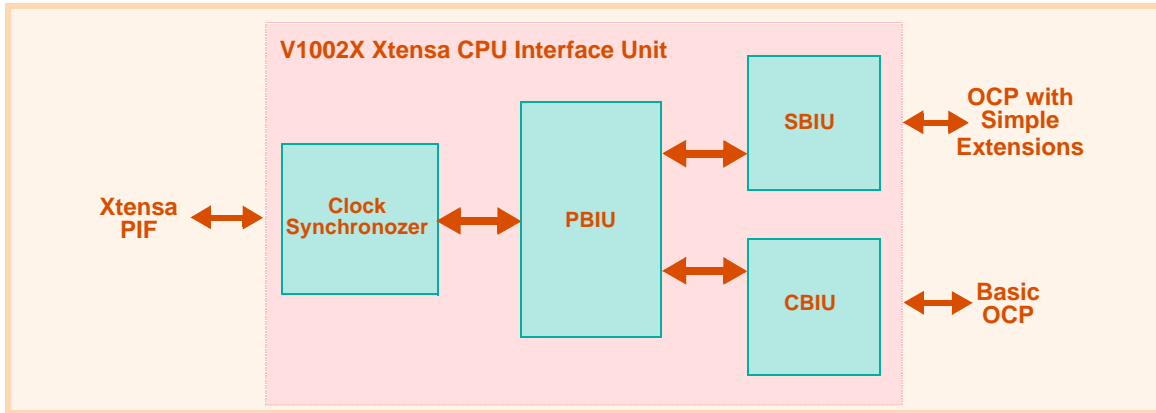


Fig 2: V1002X XIU Block Diagram

Performance

Parameter	Value	Remarks
Gate Count	11K	Approximate, for 2 peripherals.
Code Coverage	100%	Block and Arc coverage, with SureCov tool.
Technology	0.18u	Artisan TSMC
Frequency	175 MHz	Pre-route STA with Design Compiler from Synopsys.

Deliverables

- Verilog RTL
- Verification Suite
- Synthesis Scripts
- User Guide

Related Products

- V1001 - Central Control Unit with System Memory Arbiter

Target Applications

- Xtensa based SoC or ASSP, with on-chip bus different from Xtensa's PIF Bus.

Test Coverage

- TBD