



M8254APB - Programmable Interval Timer with APB Interface

Features

- AMBA APB Compatible Bus interface
- Fully synchronous, single clock edge design
- Independently instantiated three 16-bit counters
- Six software programmable counter Modes allowing the M8254APB to be used as an event counter, real time clock, digital one-shot, programmable rate generator, elapsed time indicator, square wave generator, binary rate multiplier, complex waveform generator, complex motor controller and many other applications
- High speed operation
- Counter latch and Status ReadBack command that allow the user to read the status and the count of the three counters while the count is in progress
- Binary or BCD counting

Functional Overview

The M8254APB is a programmable Interval Timer and a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software. Among them three are counters and the fourth is a control register for MODE programming. The core is compatible to standard 8254 except for bus interface. The bus interface is compatible AMBA APB which is widely used in SOC designs.

Each counter must be programmed before it can be used. Counters are programmed by writing control word and then the initial count. The Control Word Register can only be written to; status information is available with the Read-Back Command.

The three counter blocks are identical in operation. The Counters are fully independent. Each counter is a 16-bit presettable down counter. Each Counter may operate in a different mode by programming the control word register. The status of each of the counters can be read from the status register by latching the status through the status latch command. The count value of the counters can also be read by latching the count through the counter latch command.

The Read/Write Logic accepts inputs from the bus interface and generates control signals for the other functional blocks of the M8254APB. **paddr** selects one of the three counters or the control word register to be read from or written into.

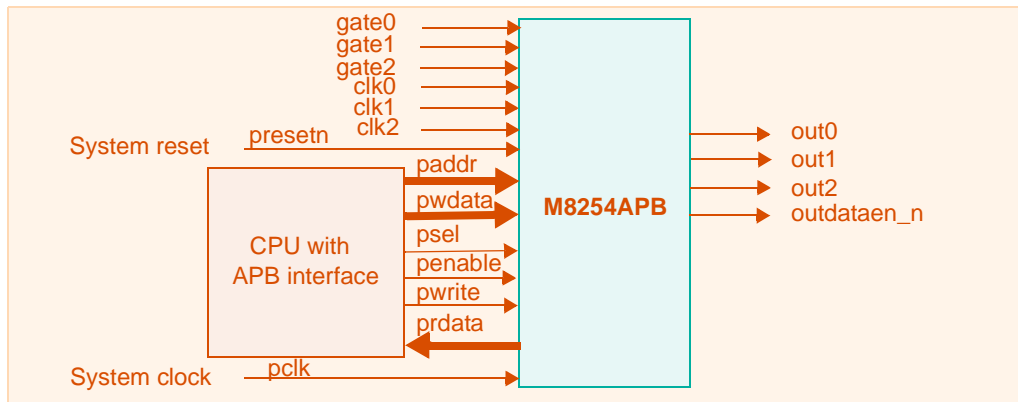


Fig.1 M8254APB in a typical AMBA system

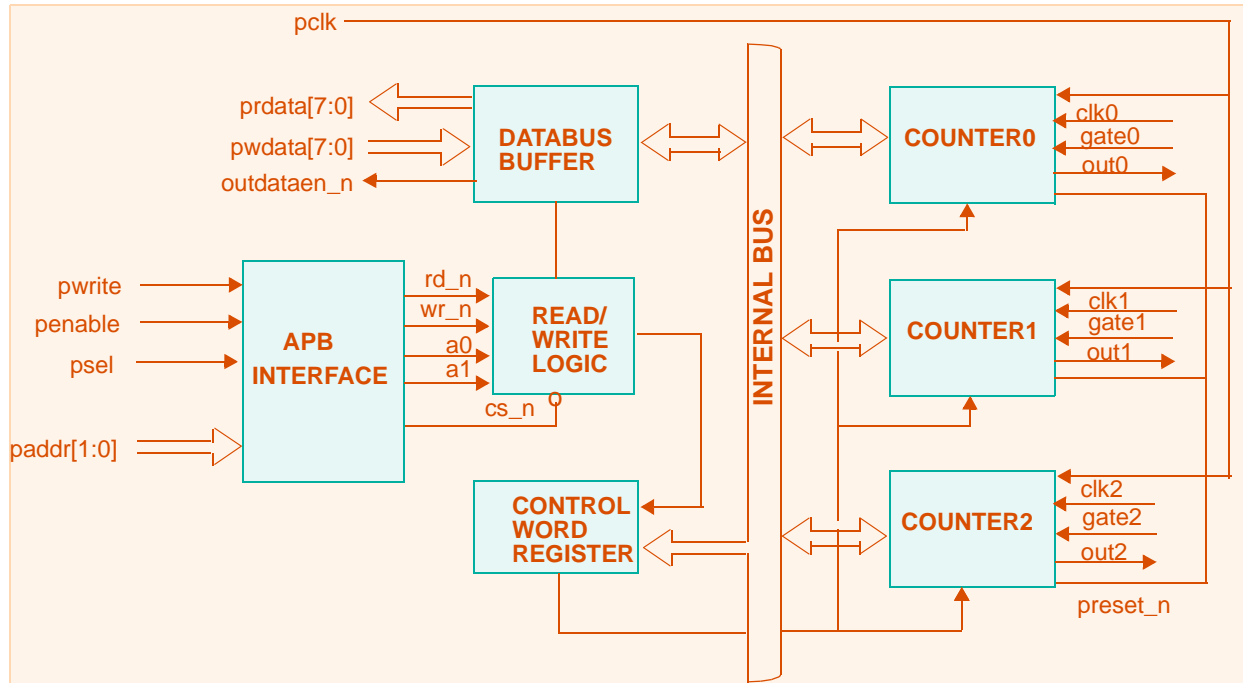


Fig.2 Internal Block Diagram of M8254APB

Performance

Parameter	Value	Remarks
Gate Count	3.9K	Without Scan Insertion
Power Estimate	24 mW	Total Average power at 150MHz
Code Coverage	99%	Block & Arc Coverage
OpenMORE Score	95	
IP Catalyst rating	TBD	
Technology	0.35	Avant! Passport Library
Frequency	150 MHz	Pre-route Simulations

Target Applications

- SOCs

Test Coverage

- Fault coverage, 94% without scan, with functional testvectors.

List of Deliverables

- User guide
- Data sheet
- Block level design document
- Verification Plan document
- Verification Description document
- Fully synthesizable Verilog source code
- Verilog test bench and test vectors
- Synthesis script for Design Compiler
- Reference technology netlist

Options

- Xilinx FPGA netlist or bitmap file for XC4000, Spartan, Virtex series

Related Products

- FPGA evaluation board
- V6001 - AHB-APB Bridge megacell

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