



M16550APB UART With FIFOs

Features

- AMBA APB interface for CPU control and data transfers
- Implements Full Asynchronous proto-col.
- 5 to 8 Bits/Character format and even/odd/no parity.
- Complete Error Detection.
- Supports Interrupt mode/ poll mode .
- Supports FIFO mode and buffer mode.
- 16x8 transmitter FIFO.
- 16x8 receiver FIFO with trigger level facility.
- Power save mode.
- 5 different maskable interrupts.
- Internal loop back mode.
- Modem handshake facility.
- Timeout interrupt.
- Line break detection.
- Fully synchronous design.

Description

M16550APB is designed to provide easy and simple interface with AMBA Advanced Peripheral bus (APB) on one side & the serial communication equipment on the other. It provides full modem handshake signals for easy interfacing with modems during communication. The design is DFT friendly.

M16550APB megacell is functionally similar to National Semiconductor NS16550A, except for the CPU bus interface. This megacell design is available as synthesizable HDL code and can be targeted to any vendors library. The gate count including FIFOs is 5.5k , when targeted to a typical ASIC library.

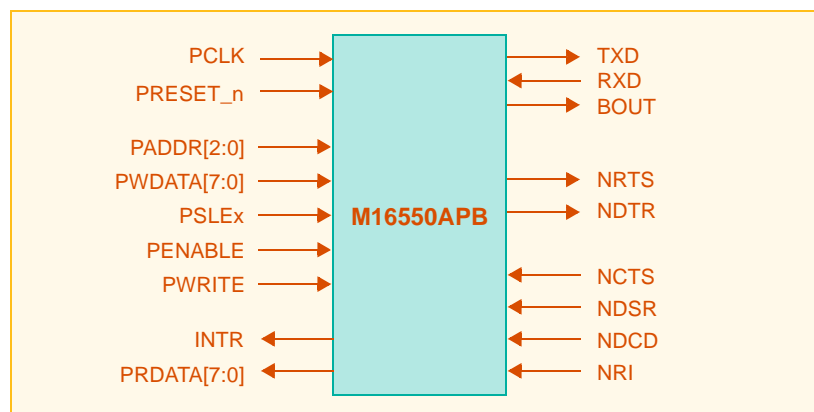


Fig 1: M16550APB Megacell Block Diagram

Services

- Design porting to FPGA including turnkey development of application software and evaluation setup.
- Core modification based on customer specification.
- Embedded design implementation on FPGA, ASIC and COT platforms.
- Custom IP development.

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